MIPI Monitoring Board

[SVL-03-UVC]

Hardware Specification

Ver.1.3

NetVision Co., Ltd.

Update History

Revision	Date	Note	
1.0	25. Feb., 2026	New File (Translation of Japanese version 1.7.)	R. Sugo
1.1	28. Apr., 2026	Changed the application name in each chapter to SVLCtl / SVLUpdater. Removed the “Applicable Versions” chapter. Updated the image showing items to check when the device is recognized as a different device, in line with the device driver update.	K.Kimura
1.2	17. Jul., 2026	Added notes/precautions regarding this board.	K.Kimura
1.3	22. Jul., 2026	Added CN1： Sub Power Connector CN1 Pin Assign. Some content has been updated to align with the Japanese version 2.0.	K.Kimura R. Sugo

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1. Overview

This document outlines the hardware specifications of the **"SVL-03-UVC",** which converts MIPI CSI-2 video signals to USB3.2 Gen2 / Gen1 or DisplayPort.

This board operates under three modes: **UVC mode, DisplayPort mode and Updater mode**, which can be set by the DIP switch (SW2).

In UVC mode, this board can capture video on a PC as a UVC (USB Video Class) compliant device. This allows for the evaluation of image sensors and the development of algorithms on various operating systems, such as Windows and Linux. Uncompressed video data can be transmitted at a maximum bandwidth of 6 Gbps. Being a UVC compliant device that does not require additional device drivers, it can be easily integrated with third-party software such as OpenCV and ROS.

In DisplayPort mode, image data from the target device can be easily displayed on a monitor in real time for verification and evaluation. The board can also be connected to an HDMI monitor using a DisplayPort - HDMI active conversion cable.

In Updater mode, the firmware and FPGA can be updated via USB. When updating, please confirm the board is start-up in "updater mode".

1.1. SVL-03-UVC Functions

UVC mode: MIPI video signals -> USB3.2 Gen2 / Gen1 (UVC) conversion
DisplayPort mode: MIPI video signals -> DisplayPort conversion
Updater mode: Update the board firmware / FPGA

1.2. Specifications (UVC Mode)

Power: USB bus supply (External power supply also available) / +5V 0.95A typ.
Input Standards: MIPI CSI-2 video signals (Data 1 - 4 lanes + 1 clock lane)
max. 1500 Mbps/Lane
Input Resolution: max. 8190 x 4095 pixel
Input Pixel Format: YUV4:2:2 (8bit), Raw8, Raw10, Raw12, Raw16, Raw20, RGB24
Output Standards: USB Video Class (UVC) Gen2 max. 6.0 Gbps, Gen1 max. 3.0 Gbps
Output Resolution: Same as the input resolution
Output Pixel Format: YUV4:2:2 (8bit), RGB24
Output Frame Rate: Any value

1.3. Specifications (DisplayPort Mode)

Power: USB bus supply (External power supply also available) / +5V 1.1A typ.

Input Standards: MIPI CSI-2 video signals (Data 1 - 4 lanes + 1 clock lane)
max. 1500 Mbps/Lane

Input Resolution: max. 8190 x 4095 pixel

Input Pixel Format: YUV4:2:2 (8bit), Raw10, Raw12, RGB24

Output Standards: DisplayPort 1.1a, max. 2.7 Gbps/Lane x4L

Output Resolution: 1280 x 720 / 1920 x 1080 / 2560 x 1440 / 3840 x 2160 / Custom resolution

Output Pixel Format: YUV4:2:2 (8bit), RGB24

Output Frame Rate: 30 FPS / 60 FPS / Any frame rate (Custom resolution)

1.4. Board Specification

Item	Content	Remark
Video Input Interface	MIPI D-PHY CSI-2 video signal	·Supports Non-Continuous / Continuous Clock. ·Standard specification: 4 data lanes + 1 clock lane. ·With customization, the following are possible: -Up to 8 data lanes + 2 clock lanes. -2 MIPI system inputs. -1 MIPI system input + 1 output.
Video Output Interface	USB3.2 Gen2 / Gen1 (Windows UVC driver) DisplayPort 1.1a	(DisplayPort mode) Dual-Mode (DP++): Not supported DPCP: None
Input Resolution	Max. 8190 x 4095 pixel	The range of widths that can be input depends on the number of lanes.
Output Resolution	Max. 8190 x 4095 pixel (UVC mode Gen2) Within 6.0 Gbps. (UVC mode Gen1) Within 3.0 Gbps. (DisplayPort mode) Within 3840 x 2160, 30fps.	(UVC mode) Dependent on the capture performance of the host PC. (DisplayPort mode) Standard supported resolution: 1280x720 / 1920x1080 / 2560x1440 / 3840x2160

			The custom resolution setting file used in SVM-06 can be used as is. (Common to both modes) It is possible to cut out any area and output it. For dot-by-dot output, the effective data rate is up to 5.2 Gbps (YUV422 8bit, using frame memory). The maximum value varies depending on the output resolution and data type.
Sync Signal		Frame Start / Frame End	
MIPI Data Lane		1, 2, 3, 4 lanes	
Data Rate Per Lane		20 ~ 1500 Mbps	Data rate per lane = Clock lane frequency x2
Supported Pixel Formats		YUV4:2:2 8bit / RGB24 / Raw8 / Raw10 / Raw12 / Raw16 / Raw20	
Other IF	I2C	1 system Frequency: 100 / 200 / 400 kHz / 1MHz (1MHz is HW only)	Voltage level follows VDDIO.
	GPIO	16bit, IN/OUT direction control for each bit, Direct connection to FPGA	Voltage level follows VDDIO.
	Synchronous Connector	Synchronous signal input and output. Direction control of IN / OUT.	Fixed at 1.8V.
Power Supply	Input Power	USB bus power / Dedicated 2pin connector	The dedicated 2pin connector has two input range selections: 5V to 5.5V / 6.5V to 16V by a jumper pin. USB bus power can be disconnected with a jumper pin. CN1: Sub Power Connector
	Output Power	VDDIO output (1.8V, 2.5V, 3.3V) 1.2V, 3.3V, 5V output	VDDIO: IO power supply setting. Shared with internal power

			supply. Current rating 1.2A (VDDIO), 1.2A (3.3V), 3.0A (5V), reserved (1.2V)
	Protection Device	eFuse 6V / 4.8A (TCKE805NL)	Recovery by turning board power OFF.
Other Functions		・Test pattern output. ・Image clipping. ・Automatically transmit I2C setting at startup from ROM. ・Virtual Channel, Embedded Line.	
Interface Connector		120pin (QSH-060-01-L-D-A)	Interface compatible with the 120pin of SVM-06.
FPGA		Artix-7 (XC7A35T) CrossLink (LIF-MD6000)	
Frame Memory		256MB (DDR3 SDRAM)	
USB	Device Controller	Infineon EZ-USB™ FX10	
	Connector	USB3.2 Gen2 Type-C	
Board Dimensions		101.6 x 101.6 x 24.0 [mm]	Length x Width x Height (Height includes spacer (10mm))
Attached Software (Windows)		NVCap, SVLCtl, SVLUpdater	
Examples of Supported Deserializer Boards		FPI-954-HF GMI-96716A-F GVI-4960-F, others	

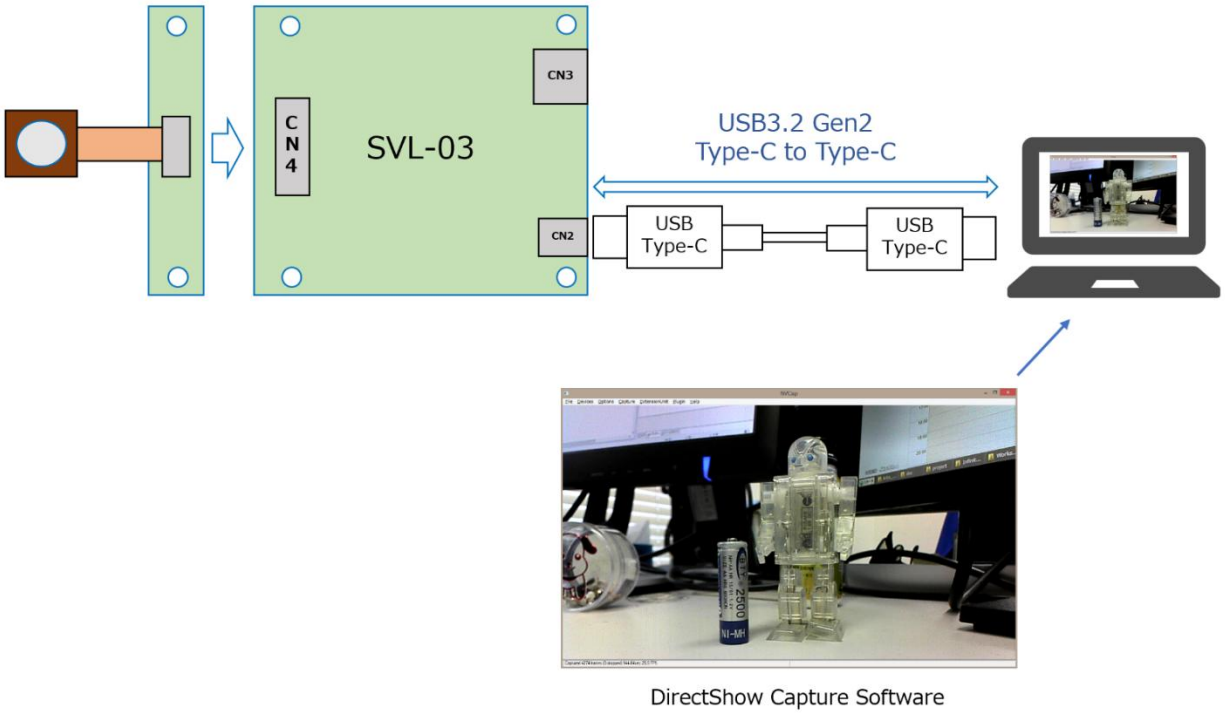
1.5. MIPI CSI-2 Data Processing Specifications

- Short Packets FS/FE are used for frame detection.
- Only payload data is sent to USB. The contents of packet header and packet footer are not sent.
- ECC and CRC errors are ignored.
- Virtual Channel supports VCX.
- When the input data exceeds the specifications of this board, the behavior is undefined.

2. UVC Mode Operation Details

This chapter describes UVC mode (MIPI input, USB output). Hardware settings are configured using the on-board DIP switches, while software settings are configured from a PC. For details on software settings, refer to the “SVLCtl Software Manual” and other related manuals.

2.1. Connection Example in UVC Mode



2.2. Setup Instructions in UVC Mode

In UVC mode, initial settings must be configured to match the specifications of the target, such as the image sensor, when used for the first time. If the settings differ from the target output, video cannot be captured correctly.

- Setting the target-side power voltage (VDDIO)

Before connecting the target device, VDDIO must be set to match the target device’s I/O voltage. VDDIO can be switched using the on-board jumper. For details, refer to the JP1 VDDIO Selection Jumper section.

- DIP switch settings

The DIP switch must be set according to the number of MIPI lanes of the target device and the USB performance of the host PC. Please refer to the SW2 DIP Switch for details.

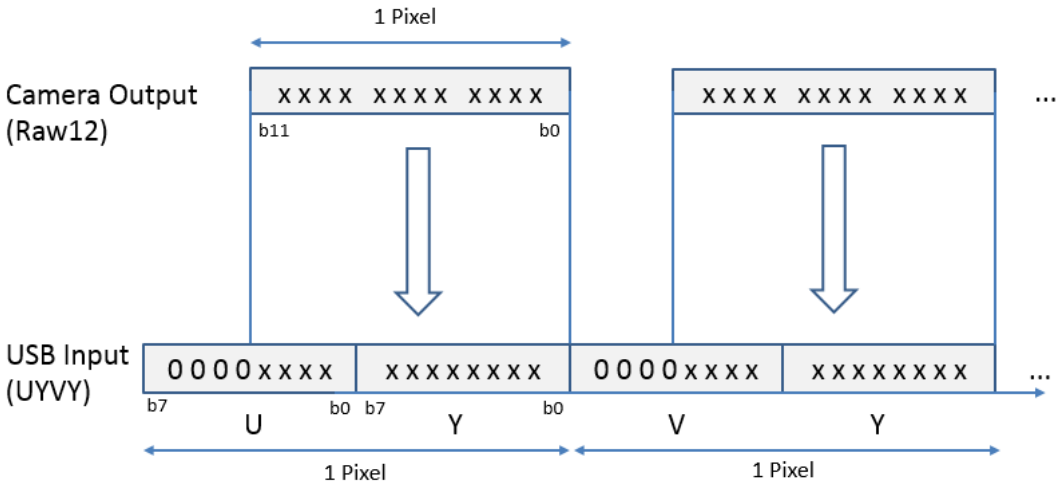
- Initial setup on a PC

Parameters and settings such as resolution, frame rate, and pixel format must be set through a PC. These settings should be set according to the specifications of the input video. If clipping is enabled, set the resolution to the value after clipping. Of the uncompressed video pixel formats commonly supported by UVC, SVLCtl can set three: UYVY, YUY2, and RGB24.

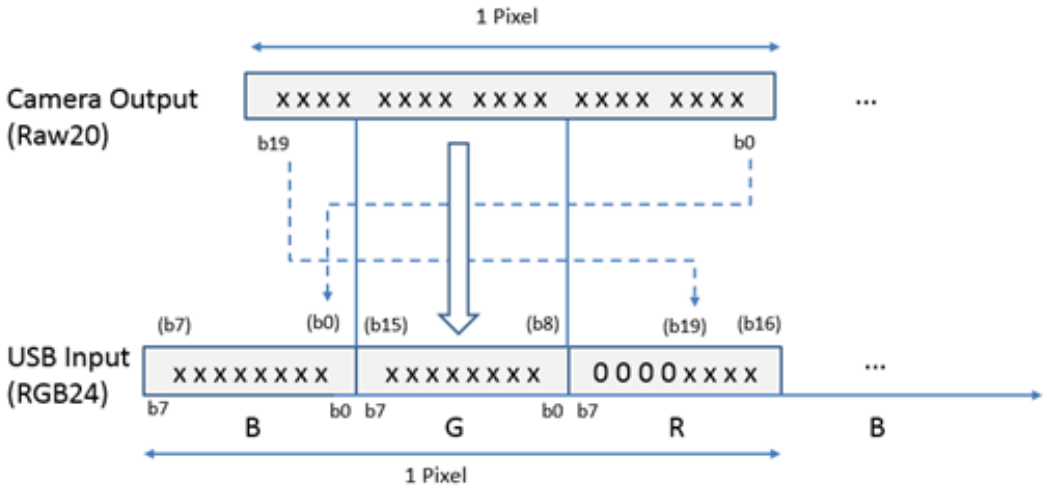
2.3. Processing for RAW Input

This board supports Raw8, Raw10, Raw12, Raw16, and Raw20 as Raw input formats. However, since the UVC standard does not support the Raw format, the device captures data using an alternative format, and Raw image processing is performed by the host PC software.

For Raw8 to Raw16 formats, the device captures data by setting the pixel format to UYVY and packing the image into 16bit per pixel. In this case, for Raw8 to Raw12 formats, the input data is expanded to a 16bit width as shown below, with the upper bits padded with 0 before being output to the PC. In addition, SVLCtl can be configured to output Raw input as a monochrome YUV 8bit format.



In the case of Raw20, the input data is treated as 24bit wide, with the upper bits set to 0 and output to the PC. Specify RGB24 in the pixel format settings, pack the images to 24bit/pixel, and import them. Then, process the raw images using software on the host PC.



The host side treats it as RGB24 and the upper bits are set to 0.

(Bit rate is 6/5 times)

2.4. Input / Output Scaling

In UVC mode, input / output scaling (Limited / Full conversion) is not performed. The input image level is not changed, and the input range is maintained when output to the PC.

2.5. Power Consumption in UVC Mode

When inputting and outputting 4K / 30FPS video without connecting a target, the current consumption is approximately 950mA for a 5V power input. If a target is connected and a video is imported, the current consumption will increase even further. Therefore, please use an AC adapter or USB cable with sufficient current capacity for power supply.

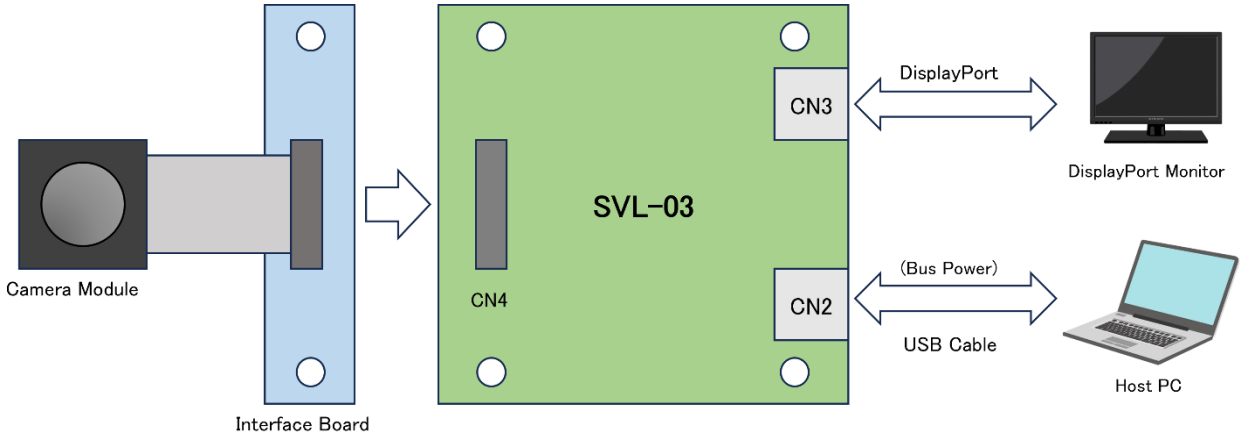
2.6. FSYNC Output Setting

FSYNC is generated by the peripheral functions of the FX10 and can be output through GPIO0-15 via the FPGA. For the pin assignments of GPIO0-15, refer to the connector specification CN4：Target Connector.

3. DisplayPort Mode Operation Details

This chapter describes DisplayPort mode (MIPI input, DisplayPort output). Hardware settings are configured using the on-board DIP switches, while software settings are configured from a PC. For details on software settings, refer to the “SVLCtl Software Manual”.

3.1. Connection Example in DisplayPort Mode



3.2. Setup Instructions in DisplayPort Mode

・ Target-side power voltage (VDDIO) setting

VDDIO must be set to match the target device’s I/O voltage before connecting the target device. VDDIO can be switched using the on-board jumper. For details, refer to the JP1 VDDIO Selection Jumper.

・ Input settings

For input settings, the number of MIPI lanes, clipping, and input pixel format must be set. The number of MIPI lanes is set using the DIP switches on the board. For details, please refer to SW2: DIP Switch.

Clipping and input pixel format are set via USB using software (SVLCtl). The clipping function is set when only a portion of the input image is output.

・ Output settings

For output settings, resolution and output pixel format must be set. The resolution is set using the DIP switches on the board. Please refer to the SW2: DIP Switch. for details. The output pixel format is set using SVLCtl.

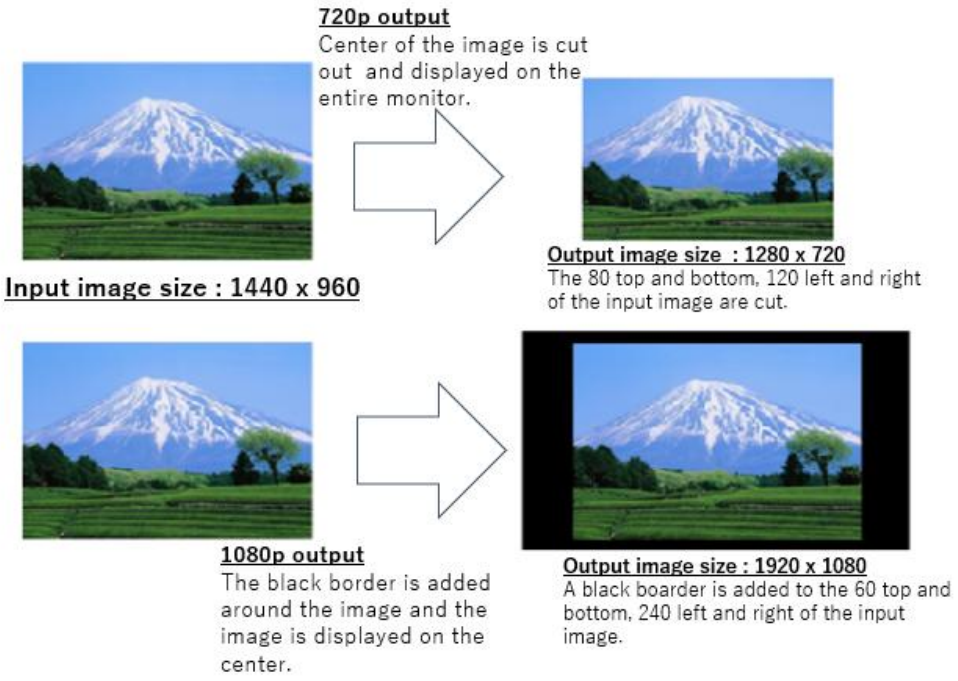
In the custom-resolution output settings, the timing of the output video signal can be specified in pixel-clock units. By writing the timing data to the board from SVLCtl, it can output at any resolution and frame rate.

3.3. Operation When Input and Output Resolutions are Different

When the input resolution is larger than the output resolution and the clipping setting is disabled, the center of the input image is automatically cropped for output. With the clipping setting enabled, the image is displayed according to the specified settings.

On the other hand, when the input resolution is smaller than the output resolution and the clipping setting is disabled, the input image is displayed in the center of the output screen with a black border around it. With the clipping setting enabled, the image is displayed according to the specified settings, also with a black border around it. The function to enlarge or shrink the image is not available.

	Output resolution smaller than input	Output resolution larger than input
Clipping Enabled	Display the clipped area according to the clipping settings.	Display the clipped area according to the clipping settings, with a black border added around it.
Clipping Disabled	Display the center area of the input image.	Display the input image at the center with a black border around it.



3.4. Processing at RAW Input

For raw input formats in DisplayPort mode, SVL-03-UVC supports Raw10 and Raw12 format inputs. When outputting a monochrome image at one pixel per output pixel (dot-by-dot), configure the grayscale-output settings in SVLCtl. At that time, only the upper 8 bits are output, and the lower bits are discarded. Raw development functions (demosaic and color rendering) are not supported.

3.5. Color Conversion Formula

The RGB and YUV conversion formula is BT.601. Input / Output scaling (Limited / Full conversion) can be set using SVLCtl.

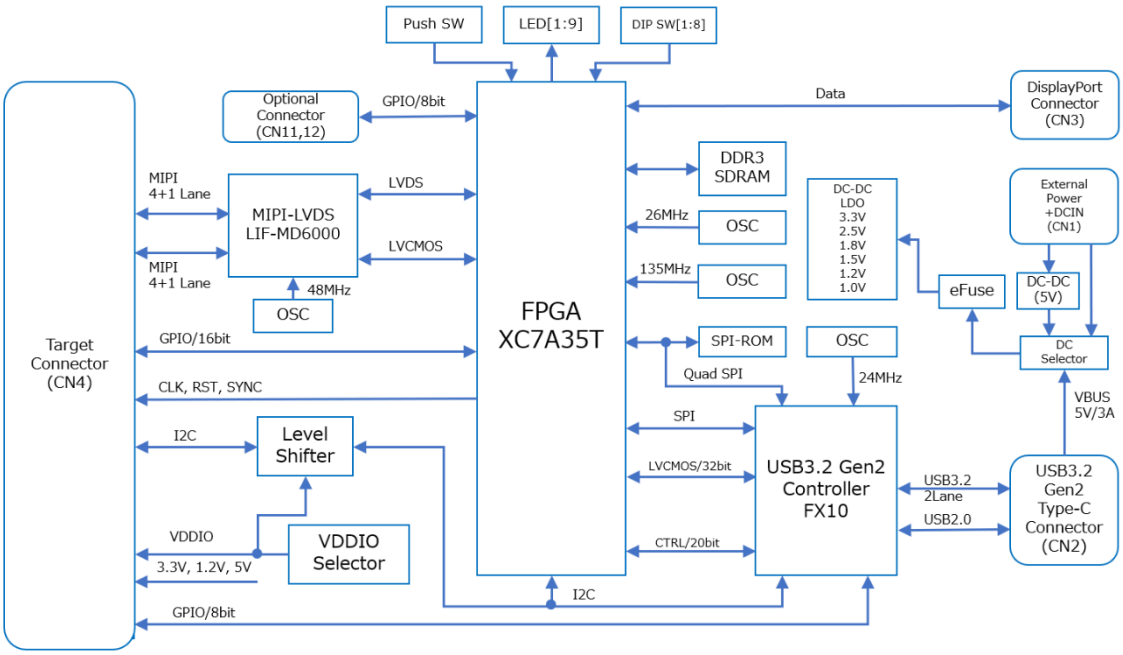
3.6. Power Consumption in DisplayPort Mode

When inputting or outputting images at 4K / 30FPS without a target connected, the current consumption is approximately 1100 mA for a 5V power input. When connecting a target and capturing images, the current consumption increases even more. Therefore, please use an AC adapter or USB cable with sufficient current capacity for power supply.

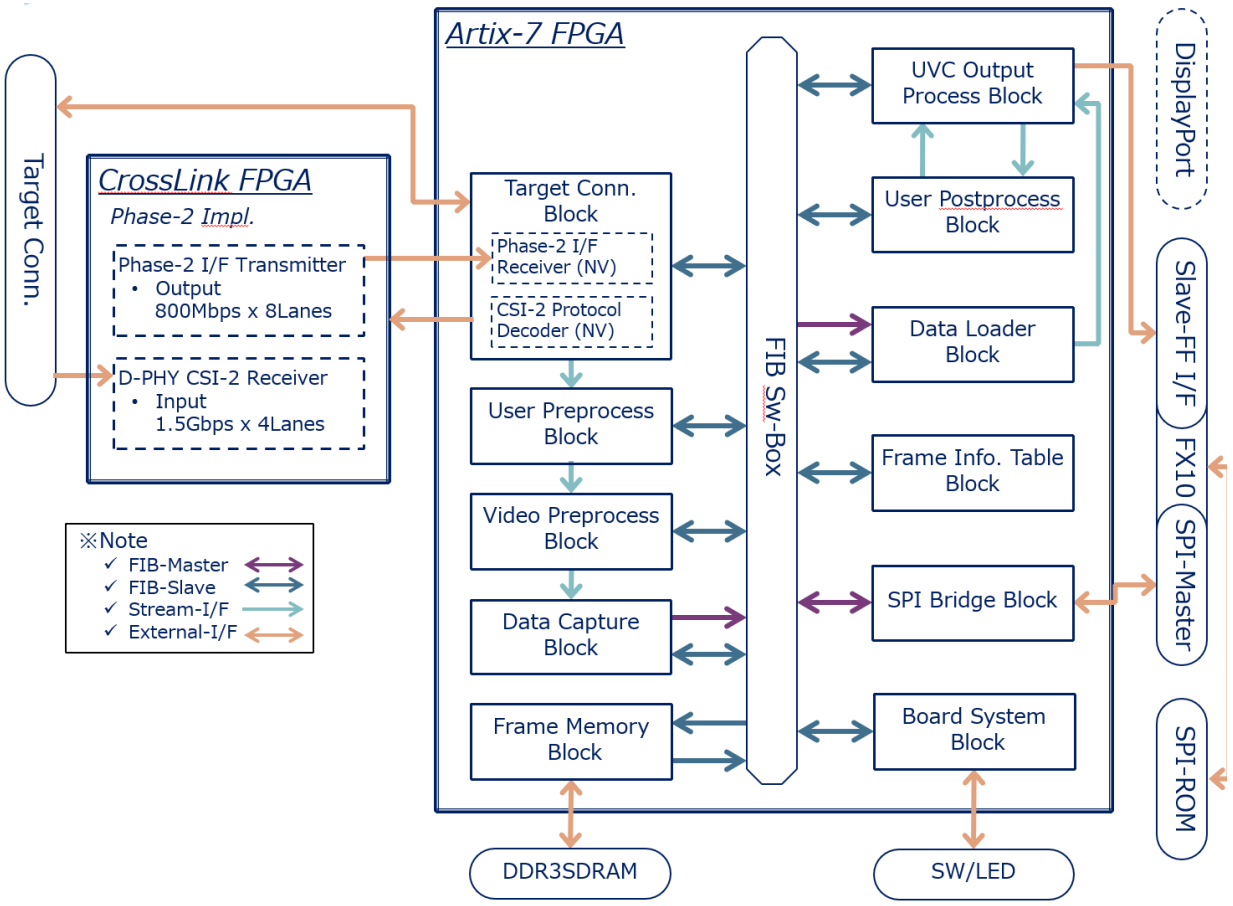
4. Block Diagram of SVL-03

The block diagrams of the SVL-03 are shown below.

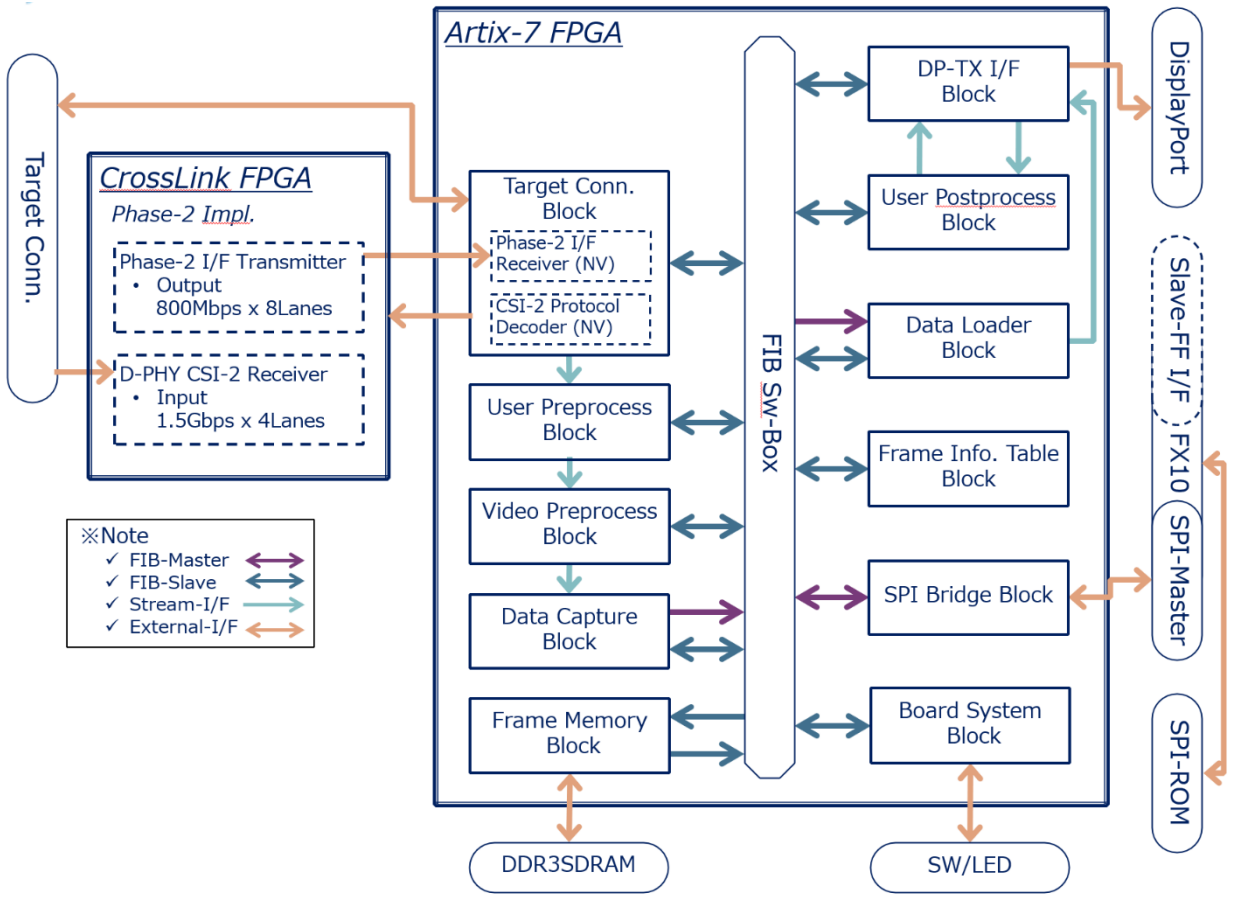
4.1. Block Diagram



4.2. FPGA Internal Block Diagram in UVC Mode



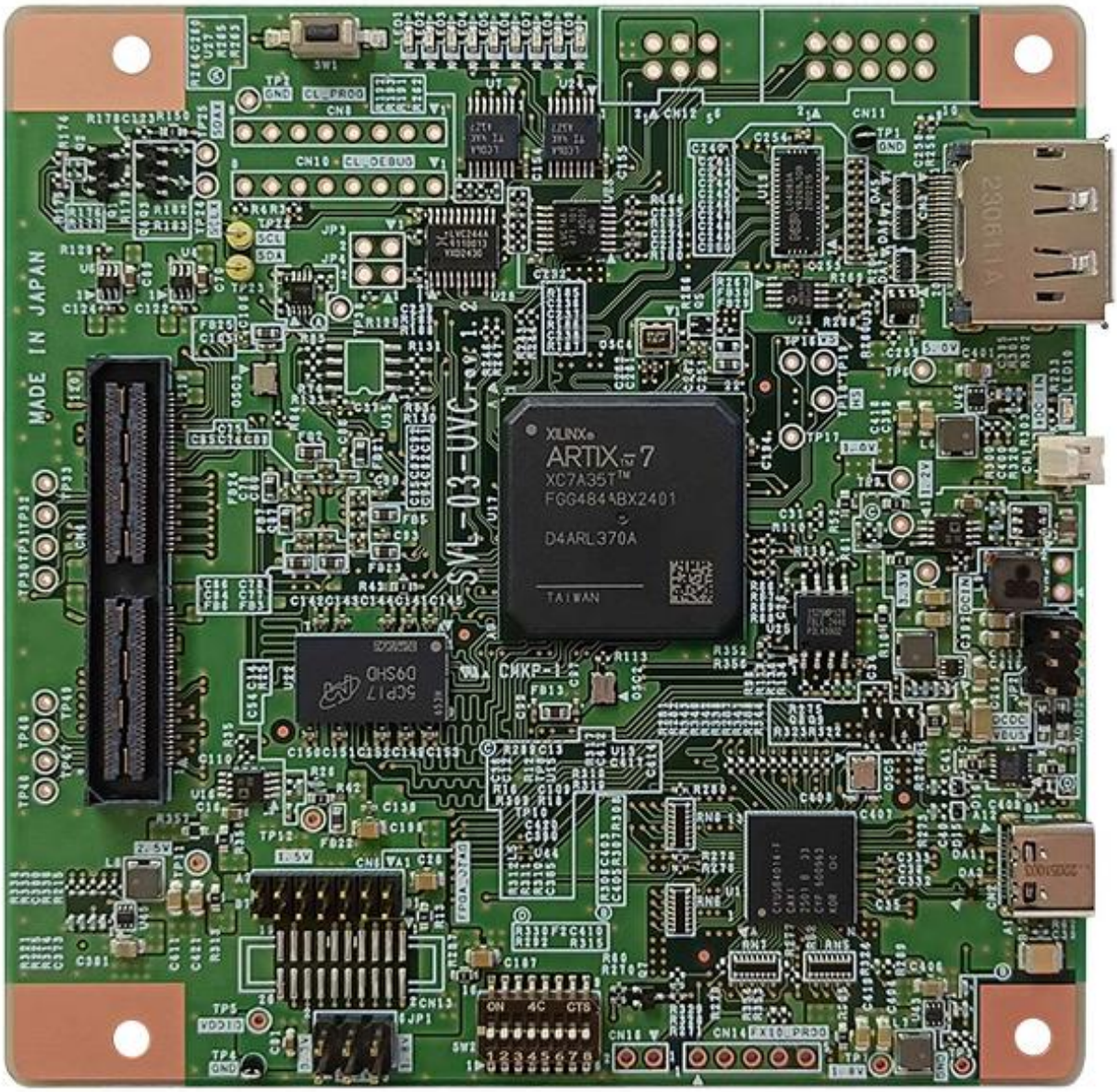
4.3. FPGA Internal Block Diagram in DisplayPort Mode



5. Board External and Dimensions

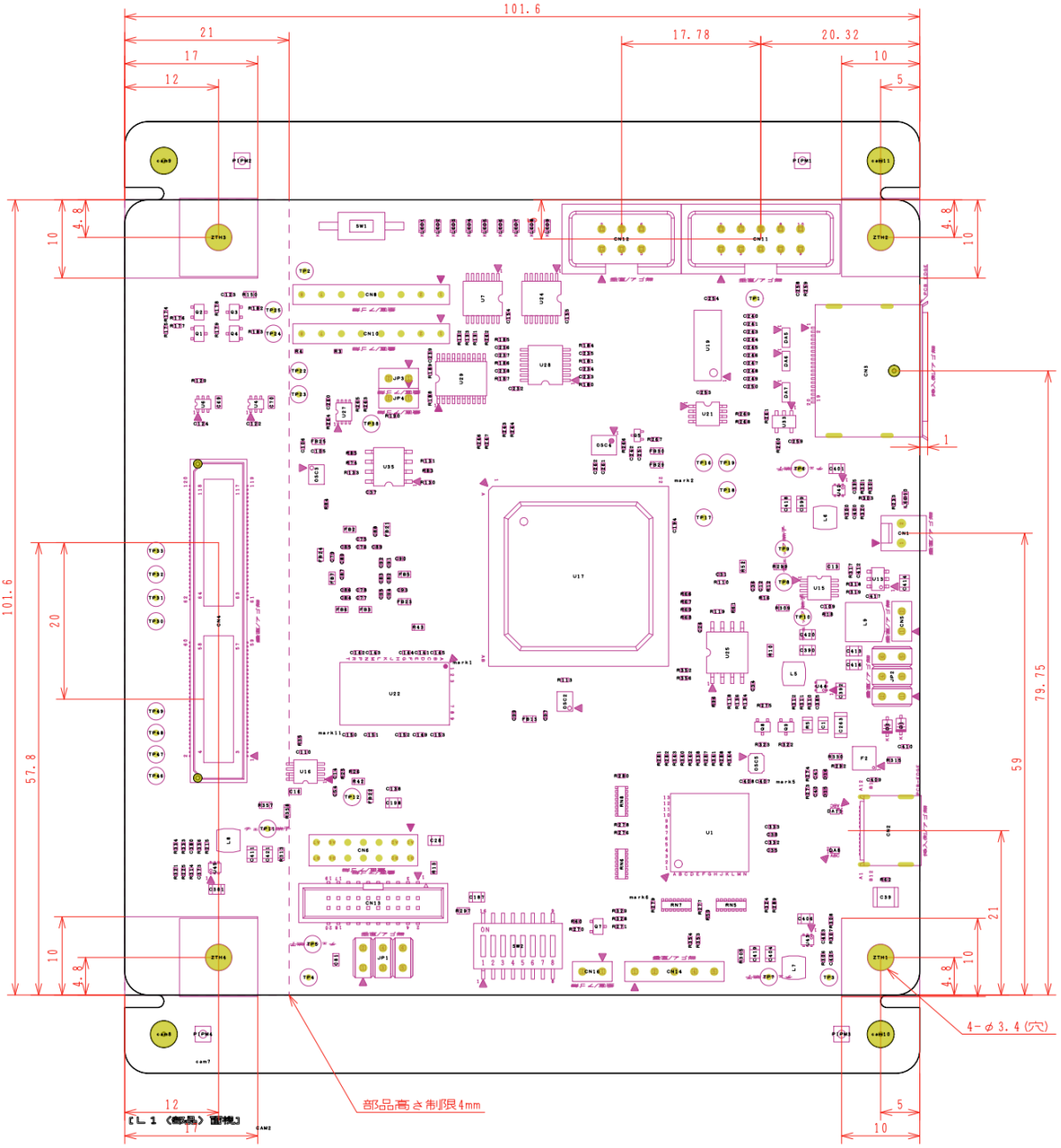
The photo and the outline diagram of the SVL-03 are shown below.

5.1. Board Photo (rev.1.2)

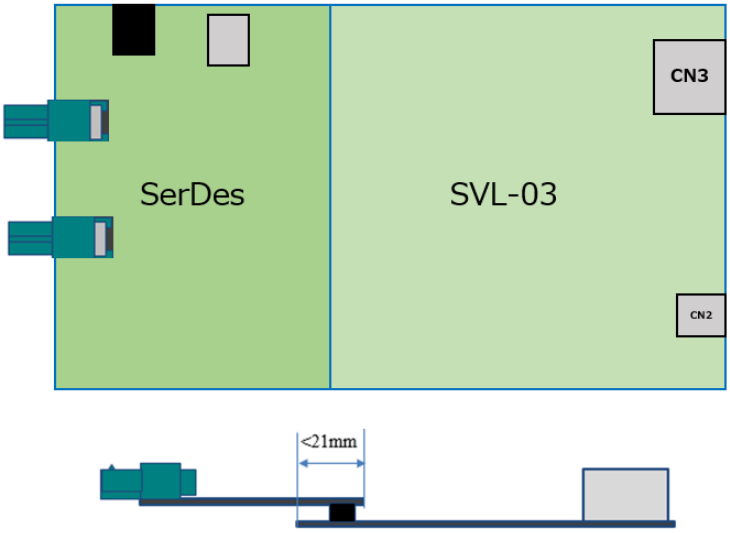


5.2. Drawing

The dimensional drawing of the SVL-03 is shown below. On the actual board, the 10 mm sections extending to the VCUT at the top and bottom are not included. The overall outline dimension is 101.6 mm, the same as our other SV series boards.

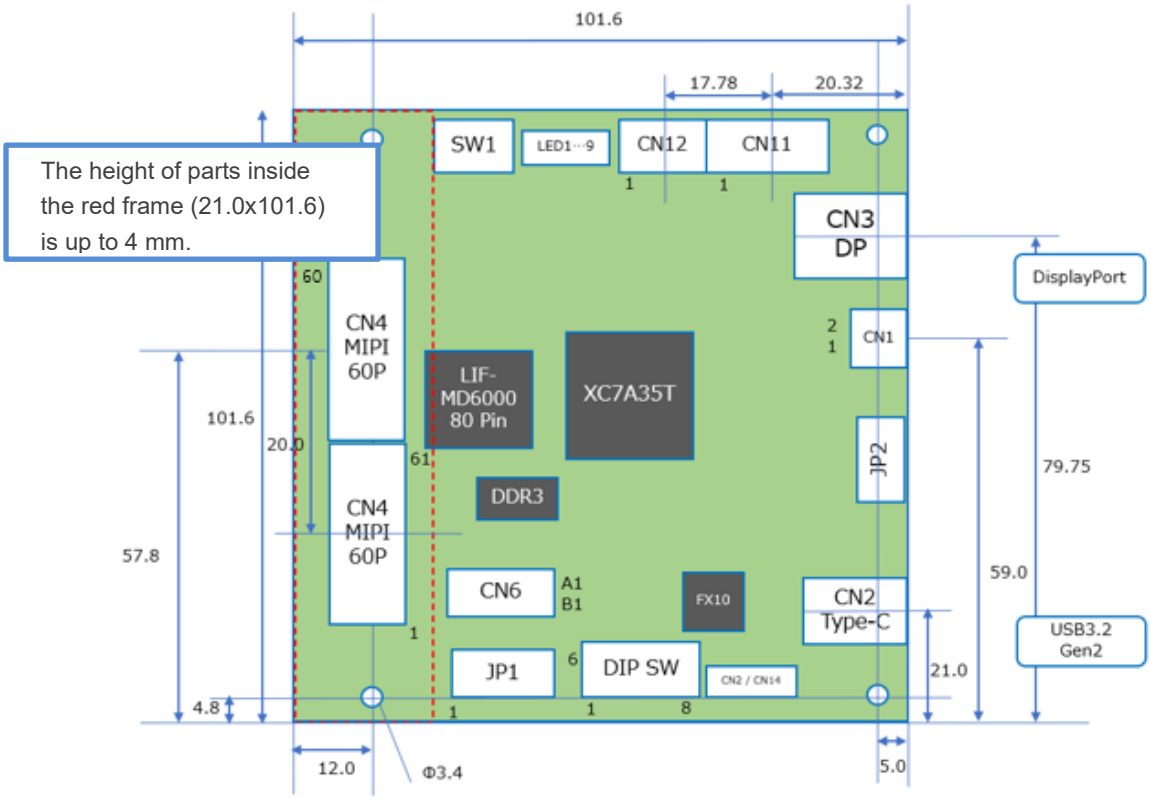


5.3. Dimensional Restriction of Connection Target Board



(Board connection example)

The SVL-03 is used by connecting a target connection board to connector CN4 as shown above. This connection board partially overlaps with the SVL-03, but the overlapping area must not exceed 21 mm from the edge of the SVL-03. This area is outlined in the red dotted box below. If using a connection board that extends beyond this frame, ensure that its shape is compatible and use a tall connector to allow proper connection of both boards.



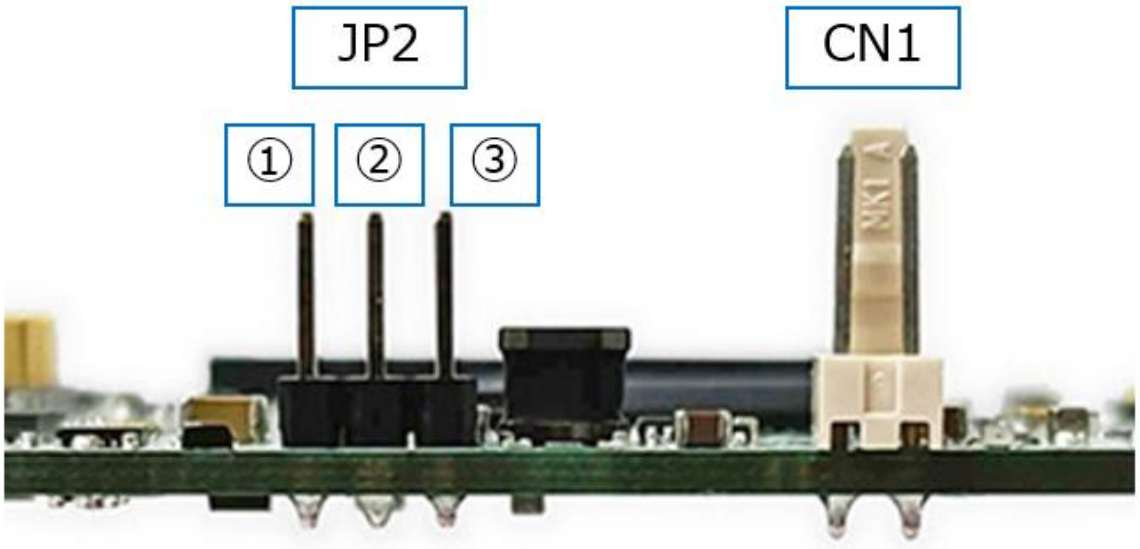
6. Connector Specifications

This chapter describes the specifications of the connectors used for normal operation when connecting to the target device.

6.1. CN1: Sub Power Connector

This power connector is used when the USB bus power is insufficient to meet the power supply requirements, or when USB bus power is not used. CN1 supports input ranges of DC5.0-5.5V and DC6.5V-16V, with the input range selected via JP2 (② and ③ in the figure below). It is also possible to disconnect the USB bus power (① in the figure below).

For DC5.0-5.5V input settings, the external power supply voltage is supplied to the board. For DC6.5V-16V input settings, the step-down circuit converts the external power supply voltage to 5V, and then it is supplied to the board. The power input is connected to the bus power (VUSB) from the USB connector via a diode OR circuit and is used as the board's internal power supply.

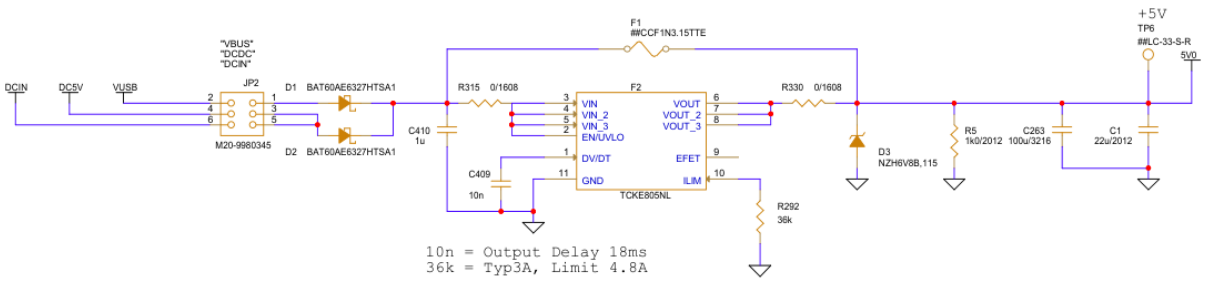


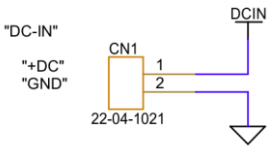
- Jumper Settings

JP2 Pin No	Open	Short-Circuit
USB Bus Power Selection ①	USB bus power is not used.	USB bus power is used as the board power supply.
DC6.5-16V Range Selection ②	DC6.5V - 16V is not used.	A voltage of 5 V converted from an external power supply by the step-down circuit is used as the board power supply.
DC5.0-5.5V Range Selection ③	DC5.0V - 5.5V is not used.	The external power supply (5.0V-5.5V) is used as the board power supply.

- Do not supply external power while both Jumpers ② and ③ are connected.
- Do not supply more than DC5.5V from the external power when jumper ③ is connected.
- At the time of shipment, jumpers ① and ③ are shorted.

- Input Power Supply Schematic.





6.2. CN2: USB Type-C Connector

This connector is a USB Type-C receptacle that connects to the host PC. Please note the following:

- Use a host PC compatible with USB3.2 Gen2/Gen1 Type-C and a Type-C to Type-C cable. This board does not support USB2.0, so it will not work with a Type-C cable, which only supports USB2.0. Please note that if connected via USB2.0, this board will be recognized as an unknown USB device.
- Type-A (host PC) to Type-C (SVL-03) cables are not officially supported by the USB I/F standard. Using such a cable may damage the host PC circuit due to overcurrent or result in insufficient power supply to the board, causing system instability.
- By using a Type-A to Type-C cable, it is possible to operate the device using by opening the USB bus power with JP2 setting and supply power from CN1. However, operation is not guaranteed in this case. For details on CN1 and JP2, refer to CN1: Sub Power Connector.

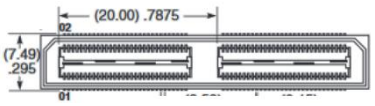
・ USB Type-C Connector Pin Assignment

Connector		1054500101					
Pin #	Signal	Direction	Description	Pin #	Signal	Direction	Description
A1	GND	-	Ground	A2	TX1+	OUT	USB3.2 differential pair +
A3	TX1-	OUT	USB3.2 differential pair -	A4	VBUS	+	Bus power
A5	CC1	-	5.1kΩ pulldown	A6	D+	I/O	USB2.0 differential pair +
A7	D-	I/O	USB2.0 differential pair -	A8	SBU1	-	Disconnected
A9	VBUS	+	Bus power	A10	RX2-	IN	USB3.2 differential pair -
A11	RX2+	IN	USB3.2 differential pair +	A12	GND	-	Ground
B1	GND	-	Ground	B2	TX2+	OUT	USB3.2 differential pair +
B3	TX2-	OUT	USB3.2 differential pair -	B4	VBUS	+	Bus power
B5	CC2	-	5.1kΩ pulldown	B6	D+	I/O	USB2.0 differential pair +
B7	D-	I/O	USB2.0 differential pair -	B8	SBU2	-	Disconnected

B9	VBUS	+	Bus power	B10	RX1-	IN	USB3.2 differential pair -
B11	RX1+	IN	USB3.2 differential pair +	B12	GND	-	Ground

6.3. CN4: Target Connector

This connector is used to connect to the target device.



Main Port

Connector	QSH-060-01-L-D-A: SAMTEC						
Pin #	Signal	Direction	Description	Pin #	Signal	Direction	Description
61	D1_N	IN	MIPI lane1 input -	62	GPIO0	IO	GPIO 0
63	D1_P	IN	MIPI lane1 input +	64	GPIO1	IO	GPIO 1
65	GND	-		66	GND	-	
67	D3_N	IN	MIPI lane3 input -	68	GPIO2	IO	GPIO 2
69	D3_P	IN	MIPI lane3 input +	70	GPIO3	IO	GPIO 3
71	GND	-		72	GND	-	
73	CLK_N	IN	MIPI clock input -	74	GPIO4	IO	GPIO 4 (Connected to TP30)
75	CLK_P	IN	MIPI clock input +	76	GPIO5	IO	GPIO 5 (Connected to TP31)
77	GND	-		78	GND	-	
79	D2_N	IN	MIPI lane2 input -	80	GPIO6	IO	GPIO 6 (Connected to TP32)
81	D2_P	IN	MIPI lane2 input +	82	GPIO7	IO	GPIO 7 (Connected to TP33)
83	GND	-		84	GND	-	
85	D4_N	IN	MIPI lane4 input -	86	GPIO8	IO	GPIO 8
87	D4_P	IN	MIPI lane4 input +	88	GPIO9	IO	GPIO 9
89	GND	-		90	GND	-	
91	SCL	IO	I2C SCL signal line	92	GPIO10	IO	GPIO 10
93	SDA	IO	I2C SDA signal line	94	GPIO11	IO	GPIO 11
95	GND	-		96	GND	-	

97	GND	-		98	NC	-	
99	GND	-		100	NC	-	
101	GND	-		102	GND	-	
103	VSYNC	IN/OUT	(Reserved)	104	GPIO12	IO	GPIO 12
105	HSYNC	IN/OUT	(Reserved)	106	GPIO13	IO	GPIO 13
107	GND	-		108	GND	-	
109	CK	OUT	Clock output	110	GPIO14	IO	GPIO 14
111	RST	OUT	Reset output (L : Reset)	112	GPIO15	IO	GPIO 15
113	GND	-		114	GND	-	
115	VDDIO	POW	IO power output	116	1V2	POW	1.2V power output
117	3V3	POW	3.3V power output	118	3V3	POW	3.3V power output
119	GND	-		120	GND	-	
MP1	GND	-		MP2	GND	-	
MP3	GND	-		MP4	GND	-	

- Lane numbers are denoted as 1-4 instead of 0-3.

Extension Port

Connector		QSH-060-01-L-D-A: SAMTEC					
Pin #	Signal	Direction	Description	Pin #	Signal	Direction	Description
1	D1_N	IN	MIPI lane5 input -	2	NC	-	(Connected to TP46)
3	D1_P	IN	MIPI lane5 input +	4	NC	-	(Connected to TP47)
5	GND	-		6	GND	-	
7	D3_N	IN	MIPI lane7 input -	8	NC	-	(Connected to TP48)
9	D3_P	IN	MIPI lane7 input +	10	NC	-	(Connected to TP49)
11	GND	-		12	GND	-	
13	CLK_N	IN	MIPI clock2 input -	14	MCU_GPIO0	IO	(Reserved)
15	CLK_P	IN	MIPI clock2 input +	16	MCU_GPIO1	IO	(Reserved)
17	GND	-		18	GND	-	
19	D2_N	IN	MIPI lane6 input -	20	MCU_GPIO2	IO	(Reserved)

21	D2_P	IN	MIPI lane6 input +	22	MCU_GPIO3	IO	(Reserved)
23	GND	-		24	GND	-	
25	D4_N	IN	MIPI lane8 input -	26	MCU_GPIO4	IO	(Reserved)
27	D4_P	IN	MIPI lane8 input +	28	MCU_GPIO5	IO	(Reserved)
29	GND	-		30	GND	-	
31	SCL	IO	I2C SCL signal line	32	MCU_GPIO6	IO	(Reserved)
33	SDA	IO	I2C SDA signal line	34	MCU_GPIO7	IO	(Reserved)
35	GND	-		36	GND	-	
37	NC	-		38	NC	-	
39	NC	-		40	NC	-	
41	GND	-		42	GND	-	
43	5V0	POW	5V power output	44	NC	-	
45	5V0	POW	5V power output	46	NC	-	
47	GND	-		48	GND	-	
49	NC	-		50	NC	-	
51	NC	-		52	NC	-	
53	GND	-		54	GND	-	
55	VDDIO	POW	IO power output	56	5V0	POW	5V power output
57	3V3	POW	3.3V power output	58	3V3	POW	3.3V power output
59	GND	-		60	GND	-	
MP1	GND	-		MP2	GND	-	
MP3	GND	-		MP4	GND	-	

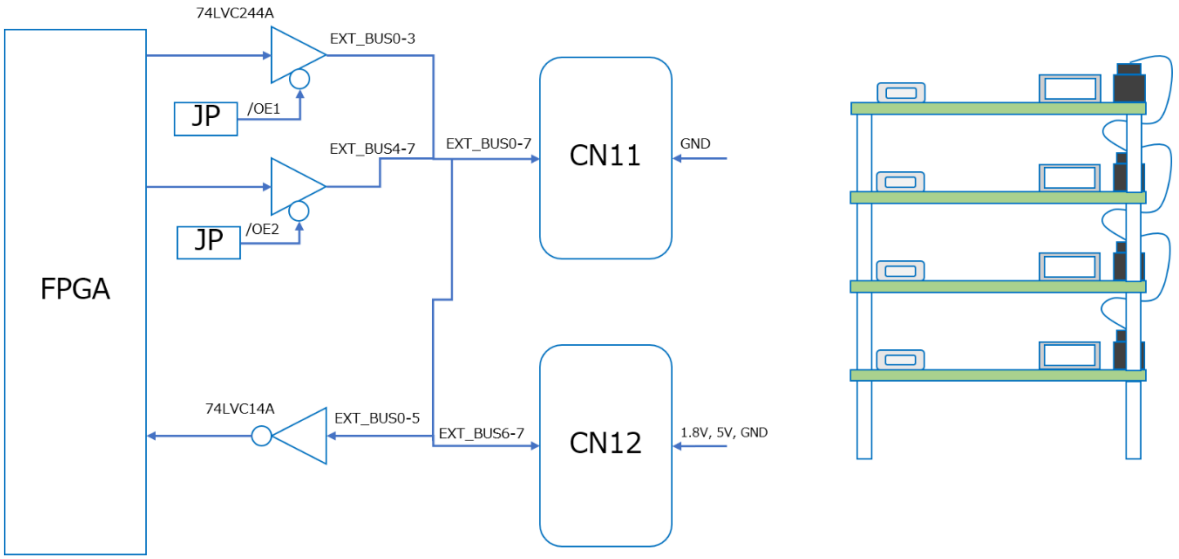
- The connector position and pin assignment are compatible with the 120pin connector of our previous boards, such as the SVM-06. Therefore, interface boards designed for our previous boards can be connected.
- MIPI lanes 5-8 are not supported in the standard version.
- If the expansion port side (1-60P) is not used, it can be treated as a 60pin connector (Connection target: QTH-030-01-L-D-A). In this case, only the main port side (61-120P) should be used.
- The HSYNC and VSYNC pins are reserved for customization and have no function in the standard version.

- The default state of GPIO pins is Hi-Z (FPGA internal pull-up). The direction and level of each pin are set by FPGA registers.
- The IO voltages for each single-ended port of the FPGA are determined by jumper JP1.
- The MCU_GPIO pin is a reserved function. The default state of this pin is Hi-Z.
- The clock output frequency is set using our software “SVLCtl”.
- SCL and SDA are connected to the I2C bus inside SVL-03 via a level conversion circuit.
- GPIO pins are controlled via FPGA registers.
- Do not input signals with voltages exceeding VDDIO to the board.

6.4. CN11-CN12 Connector for Synchronous Wiring

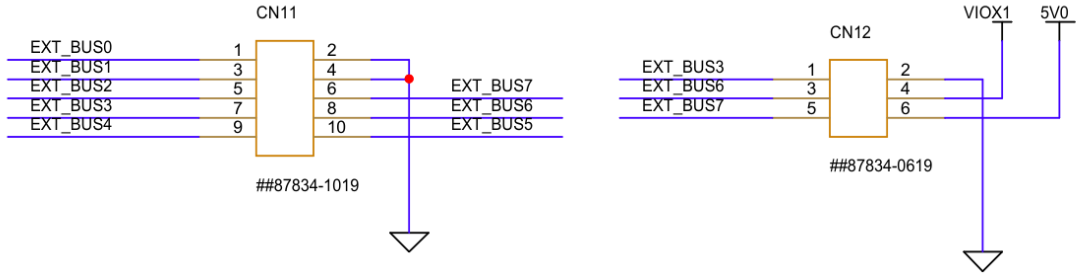
The CN11 and CN12 connectors are used for synchronous wiring between boards, using 2.54 mm pitch IDC connectors. For custom features, these connectors can be used to connect multiple boards for capture synchronization and time-stamping functions. They are not used in the standard version.

- Block Diagram



When JP3 on the board is shorted, the EXT_BUS0-3 signal lines are in output status. When JP4 is shorted, the EXT_BUS4-7 signal lines are in output status.

- Pin Assignment



7. Component Details

7.1. SW1: Push Switch

SW1 is used to output a reset signal or retransmit the initial register settings. The function of this switch can be configured via SVLCtl.

7.2. SW2: DIP Switch

SW2 is an 8bit switch used for setting the various operating modes of SVL-03. The board can be set to the following settings.

No. #	Item	OFF	ON
1	USB3.2 Gen2 / Gen1 connection selection (UVC mode only) DisplayPort output frame rate setting (DisplayPort mode only)	Auto (Gen2 or Gen1 auto configuration) (Determined when started in UVC mode) 60FPS (DisplayPort mode)	Gen1 fixed connection (Started in UVC mode) 30FPS (DisplayPort mode)
2	Test pattern output	Standard operation	Test pattern output
3	Input lane setting	3: ON, 4: OFF -> 1 Lane 3: OFF, 4: ON -> 2 Lane 3: ON, 4: ON -> 3 Lane 3: OFF, 4: OFF -> 4 Lane	
4			
5	Monitor output resolution setting (DisplayPort mode only)	5: OFF, 6: OFF -> 1080p (1920 x 1080) 5: ON, 6: OFF -> 4k (3840 x 2160, 30fps only) 5: OFF, 6: ON -> 720p (1280 x 720) 5: ON, 6: ON -> 1440p (2560 x 1440) or (Custom resolution)	
6			

7	Mode selection (Startup)	7: OFF, 8: OFF -> DisplayPort mode 7: ON, 8: OFF -> Updater mode 7: OFF, 8: ON -> UVC mode 7: ON, 8: ON -> (Reserved)
8		

The table below shows the connection status of the PC and cable combination when the Gen2 / Gen1 connection selection is set to Auto.

	PC (host) Gen2 Connector	PC (host) Gen1 Connector
USB3.2 Gen2 cable	Gen2	Gen1
USB3.2 Gen1 cable	Gen1	Gen1

- Using Gen2 settings, please check if the PC and cable are compatible with Gen2.
- Some additional settings need to be made on SVLCtl.
- The connection status can be checked on SVLCtl.
- In DisplayPort mode, the USB Gen2 / Gen1 Auto connection is fixed.

7.3. LED1-9: Operating Status Indicator

These LEDs display the operating status of the board or FPGA. After a successful startup, the LEDs operate as follows.

LED #	Description
1	Lights up to indicate that the power supply to the target is active. (Red LED)
2	Lights up to indicate that the clock supplied to the target is locked.
3	Lights up to indicate that the sync signal from the target has been successfully decoded.
4	Lights up at a cycle that divides the VSYNC (FS/FE after MIPI decoding) from the target by 3.
5	(DisplayPort mode) <Reserved> (UVC mode) Lights up when UVC transfer cannot keep up and frames are dropped due to buffer overflow.
6	<Reserved>
7	<Reserved>
8	Lights up when data is being loaded from frame memory.

9	(DisplayPort mode) Turns ON/OFF the VSYNC synchronization signal to the DisplayPort monitor output at a cycle divided by 3. (UVC mode) Turns ON/OFF the VSYNC synchronization signal to the UVC output at a cycle divided by 3.

- The LEDs labeled as <Reserved> above may be assigned functions in the future. In the current version, their lighting status varies depending on the internal state of the board.

7.4. JP1: VDDIO Selection Jumper

JP1 is used to select the IO power supply (VDDIO) for the target device from the SVL-03. The available options are 1.8V, 2.5V, and 3.3V.

VDDIO is intended to be used as an IO power supply voltage for the target device. Additionally, GPIO0-15, CLK, RST and SCL / SDA signal lines operate at the VDDIO voltage level.

7.5. JP2: Board Power Setting Jumper

For details, please refer to CN1: Sub Power Connector.

7.6. JP3-JP4: Synchronous Connector Jumper

For details, please refer to CN11-CN12: Connector for Synchronous Wiring.

7.7. Operating Temperature Range

The operating temperature range of the ICs on the SVL-03 is 0-80℃. However, this value does not account for heat generated by the devices themselves. When capturing high-bandwidth video, such as 4K / 30fps, consider attaching a heatsink to the FPGA or using a cooling fan to keep the IC die operating within the 0-80°C range.

For reference, when an LPD25-15B (25 x 25 x 15mm) heatsink is attached to the FPGA and used in an open space with natural air cooling, the calculated upper operating temperature limit is 35°C in UVC mode 30°C in DisplayPort mode (measured values in our test environment). We have confirmed that the device will operate at temperatures above this limit, but we cannot guarantee that it will function properly.

8. Check Terminal

Do not use any test points other than TP1-TP5, as doing so may cause damage to the board.

8.1. TP1-4: GND

These are used as GND (ground) terminals.

8.2. TP5: VDDIO

This is used to verify the voltage of VDDIO.

9. Notes

To ensure proper use of this board, please follow the precautions below:

1. Turn off the power to this board before connecting or disconnecting the interface board or target.
2. Do not input any external signals when this board is not powered.
3. Use a power supply with sufficient current capacity to ensure stable operation.
4. Turn on the power to the board only after the upstream device has stopped sending signals.
5. Please use the latest versions of SVLCtl and SVLUpdater.
6. When inputting signals from an external device, be careful that the voltage does not exceed the VDDIO voltage of the board.
7. If the board is enclosed in a case, consider using a heat sink or cooling fan for proper operation.
8. The contents of this document are subject to change without notice.
9. Reproduction of this document, in whole or in part, without permission is strictly prohibited.
10. Please note that if any modification or rework is performed on this board, such as changes to components or cables, the board will no longer be covered by the warranty.
11. If you suspect a defect or observe any malfunction with this board, please contact us or the distributor from which the board was purchased.

10. Appendix

10.1. Frame Drops or Image Distortion in UVC Mode

- Check that the PC's Type-C port and the cable are USB3.2 Gen2 compatible.
- Set Frame Memory to "ON" via the board configuration software SVLCtl.
- In the PC settings, open Control Panel -> System and Security -> Power Options and set the power plan to "High Performance". If the PC is a laptop and the option is not available, open System -> Power & Battery and set the power mode to "Optimal Performance".

10.2. When Recognized as an "Unknown USB Device"

If the board is connected to a PC using a Type-C cable that only supports USB2.0, it will be recognized as an "Unknown USB Device". Be sure to use a Type-C cable that supports USB3.2 Gen2.

· Device Manager screen when connected via USB2.0.

10.3. When Recognized as an "Other Devices"

If the board is recognized as an "Other Devices", please install the device driver. The device driver is included in the "SVL-03-UVC full package" which can be downloaded from our product support page. Please install the device driver as described in the manual.