USB3.0 Video Capture Board

(SVP-01-UVC)

Hardware Specification

Rev. 1.3

NetVision Co., Ltd.

Update History

Revision	Date	Note	
1.0	30. Sep., 2022	New File (Translation of Japanese edition ver.1.3)	R.Sugo
1.1	16. Jan., 2025	Change the product name from “SVP-01-U” to “SVP-01-UVC”.	R.Sugo
1.2	18. Feb., 2025	Corrected the description of RGB888 in “SW2: DIP Switch” in chapter 6.3.	R.Sugo
1.3	14. Aug., 2026	Revised and updated based on the Japanese version 2.1.	R.Sugo

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1. Outline

This document is a hardware specification of the **"SVP-01-UVC"**. SVP-01-UVC is a board for capturing video signals output from an image sensor with USB3.0 connection, and displaying on an external monitor with DisplayPort connection.

This board has three modes; **UVC mode**, **DisplayPort mode** and **Updater mode**.

In UVC mode, the device can be captured from a PC as a UVC (USB Video Class) camera, allowing image sensor evaluation and algorithm development on various operating systems such as Windows and Linux. The board can operate using USB bus power, but if the USB power supply is insufficient, provide +5V to the power connector on the board.

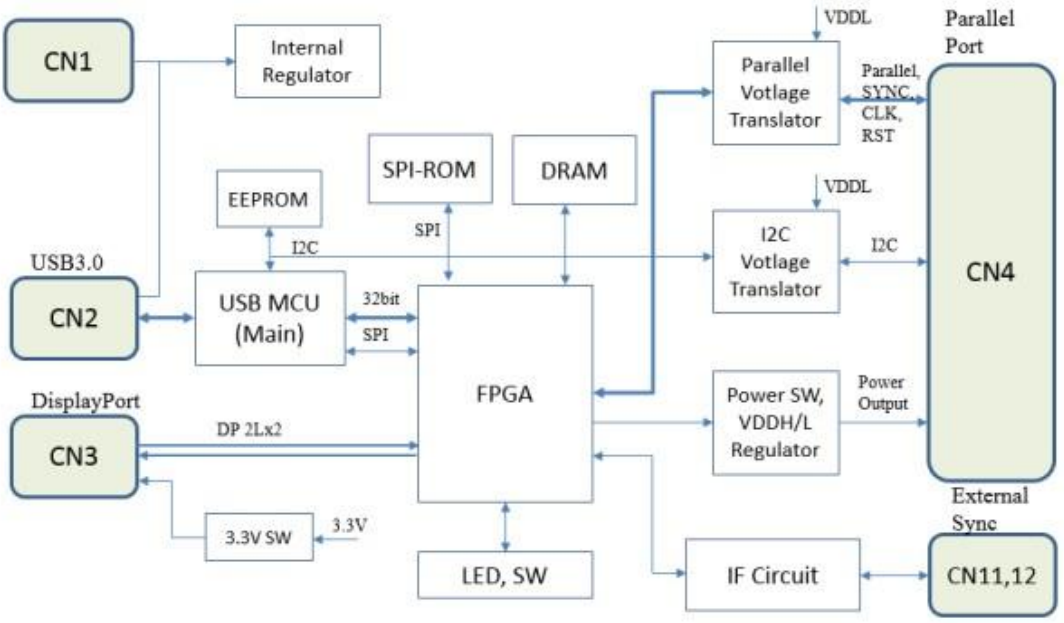
Video data is transferred to the PC via USB3.0, so this board supports uncompressed video data with a bandwidth of up to 3Gbps. The device driver is unnecessary for video capturing, making it easy to connect to third party software such as OpenCV or ROS. (When changing the board settings, it is necessary to install the driver.)

In DisplayPort mode, the received video can be output to an external LCD monitor using a DisplayPort cable. Connection to an HDMI monitor is also supported by using a DisplayPort - HDMI active conversion cable.

In Updater mode, the firmware of on-board devices such as the microcontroller and FPGA can be updated via USB. UVC mode does not support board updates, so be sure to start the board in Updater mode when performing an update.

Each mode can be selected by the startup states of DIP switch (SW2) #7 and #8 on the board. The board operates in UVC mode when #7 = OFF and #8 = ON, in DisplayPort mode when #7 = OFF and #8 = OFF, and starts in Updater mode when #7 = ON and #8 = OFF.

1.1. Block Diagram



1.2. Specification

- Power : USB Bus Supply (External Power Supply can also be used.)
  - Supply voltage: +5V (4.75V - 5.5V)
  - Operating current (typ): 0.72A (DisplayPort) / 0.6A (UVC)
- Input Format (Via CN4, 5):
  - Parallel video signal (PCLK / VSYNC / HSYNC; Embedded Sync (BT.656) Supported.)
    - PCLK < 150MHz
    - Input bit width: 8bit / 16bit / 24bit / 32bit
    - Input pixel format: YUV4:2:2 (8bit), RGB24, RAW
    - IO voltage (VDDL) level: 1.8V - 3.3V
- Frame Memory: 256MB
  - Only when the frame memory usage setting is enabled.
- Input Resolution: Up to 8190 x 4095 pixel (4094 x 4095 at 8bit)
  - Input image can be clipped in any area.
- USB output: USB3.0 (Operating in USB Video Class)
  - Operating USB2.0 HS (480Mbps) is possible.
- DisplayPort Output: DisplayPort 1.1a
  - Raw bit rate = 2.7Gbps / Lane x 2L (Throughput 4.3Gbps)

- Dual-Mode (DP++): Incompatible
- DPCP: None
- Output pixel format: RGB24, YUV 4:2:2 (8bit)

・ Power Output: IO voltage x1, Target voltage x2

・ Serial Communication: I2C (max. 400kHz, device address 7bit)

- IO voltage is the same as voltage level of video signal (VDDL).

・ Reset Signal Output

・ Clock Signal Output

・ GPIO Input / Output (Video signal + GPIO = Up to 32bit)

- By mounting connector CN5, 32bit can be used.

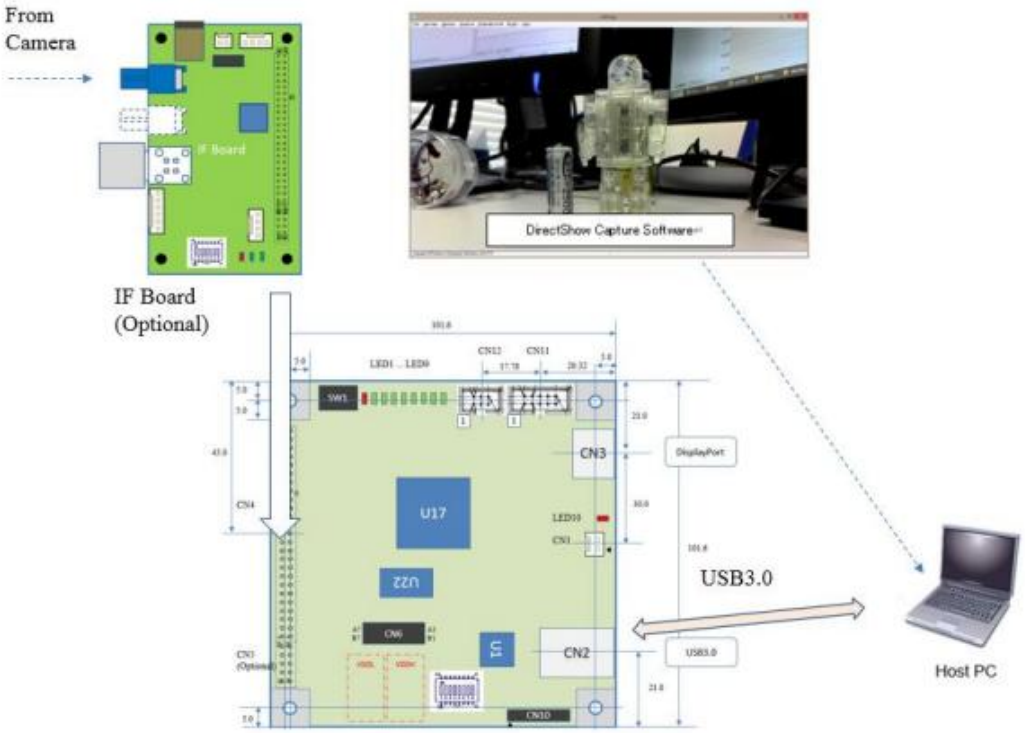
・ USB Device Name

- UVC mode: “SVP-01U”
- When a board ID is assigned, a number such as “(1)” is appended to the end of the board name.

2. UVC Mode Operation Details

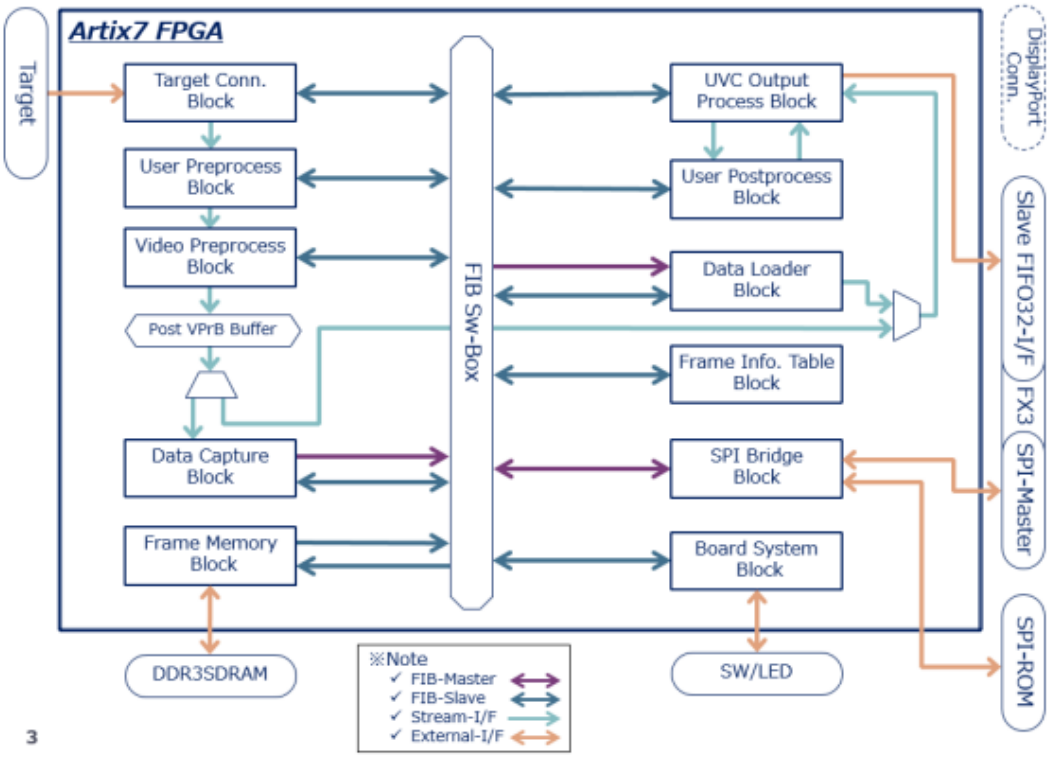
This chapter describes the UVC mode. The SVP-01-UVC starts in UVC mode when powered on with DIP switch (SW2) settings #7 = OFF and #8 = ON.

2.1. UVC Mode Connection Configuration Example



- USB connector supplies power to this board.
- If the host PC does not have supply capacity enough, supply +5V from CN1.

2.2. FPGA Internal Block Diagram in UVC Mode



2.3. Format Setting

In UVC mode, the required settings are the resolution, frame rate, output pixel format configuration, and synchronization signal settings. These settings are written via USB connector with SVMCtl. Once the initial configuration is completed, no further settings are required from the second startup onward.

Set the resolution and frame rate according to the specifications of the input video. When outputting only a specific region of the input image, configure the clipping settings. If clipping is enabled, set the resolution to the clipped output resolution.

For parallel video signals, set the synchronization-signal polarity appropriately. On this board, the polarities of VSYNC, HSYNC, and DE (when used) can be configured as needed. When inputting embedded sync signals in the BT.656 format, enable the embedded sync setting.

The output pixel format is set according to the input pixel format of the video signal. Among the uncompressed video pixel formats commonly supported by many operating systems, the formats configurable in SVMCtl are UYVY, YUY2, and RGB24. For RAW format, it can be set as UYVY or YUY2 format and displayed in grayscale or color with the display plug-in of the capture software (NVCap). If support for additional

output pixel formats is required, customization will be necessary. Please contact us for further assistance.

The bus width of the input signals is set from 8bit - 32bit with DIP switch setting. For RGB24 input, 24bit / pixel is supported.

2.4. Automatic Frame Rate Adjustment According to USB Transfer Bandwidth

The USB3.0 transfer bandwidth (theoretical value) is up to 3Gbps, and the USB2.0 HS transfer bandwidth is 480Mbps, but the input signal band supports higher data rates. Also, the actual usable USB bandwidth varies depending on the host controller and operating environment.

By enabling the automatic frame rate adjustment function, the output frame rate is automatically adjusted to match the effective USB bandwidth, and it is possible to capture video signal input in throughput that exceeds the USB bandwidth. This feature can be enabled by selecting "Auto" for the "Decimation" setting in SVMCtl and then restarting the board. When input video signals exceed the available USB transfer bandwidth at peak load, this feature must be enabled. Enabling it, the frame memory also enables and increases the latency of data.

If the USB output is not completed in time and the frame memory is full, the newly input frames are discarded.

2.5. UVC Mode Setting

As mentioned above, UVC mode requires initial setting according to the specifications of the image sensor at first use. If the setting is different from the output of the image sensor, it cannot be captured properly.

1. Target side power supply voltage (VDDH, VDDL)

Before connecting the target device, VDDL must be set to match the IO voltage of the target device. Since VDDH supplies the power voltage to the target device, configure it according to the device's requirements.

VDDL / VDDH can be switched by VR on the board. It is set to 3.3V at the time of shipment.

2. DIP switch

It is necessary to set the DIP switch according to the bit width of the target device. See "SW2: DIP Switch" for the setting. It is set to 8bit at the time of shipment.

3. Initial setting from the PC

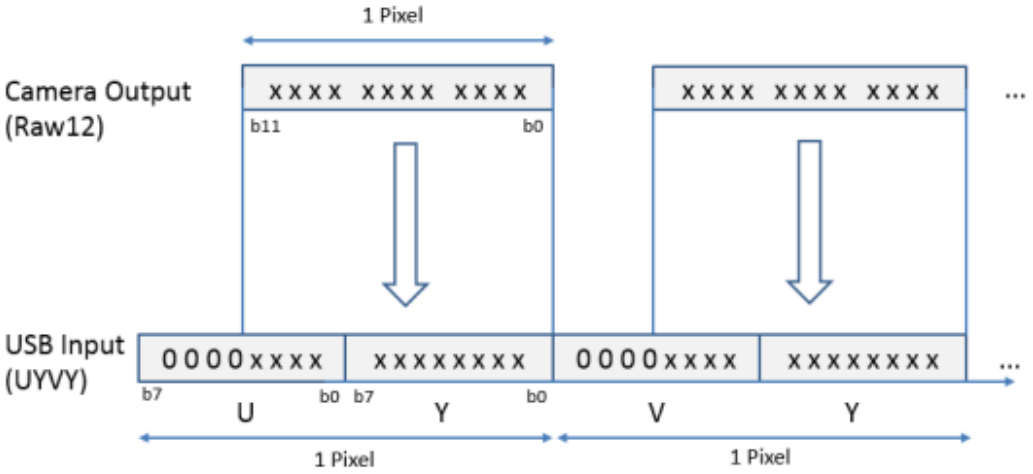
It is necessary to make initial settings such as resolution and pixel format with the PC. These settings are performed using the setup software “SVMCtl”, which can be downloaded from our website. For instructions on operating SVMCtl, refer to the “SVMCtl Software Manual”.

- SVMCtl may be updated from time to time. Please download the latest version from our website.
- SVMCtl can only support Windows (after Windows7) environment.
- This board is recognized capture device with the name “SVP-01U” by a PC.
- If you assign a device number with SVMCtl, the ID number is added after the device name.

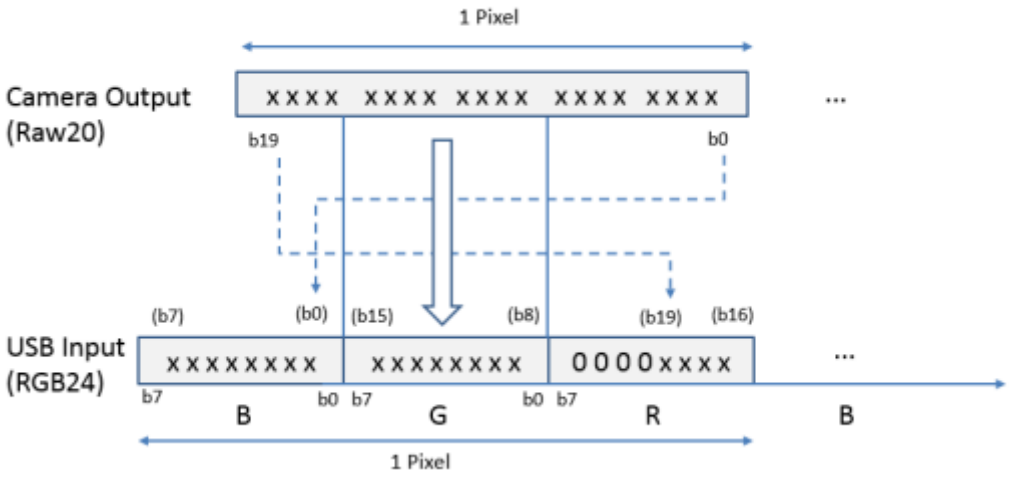
2.6. Processing at RAW Input

For RAW output image sensors, the UVC mode supports RAW8 / RAW10 / RAW12 / RAW16 / RAW20 formats. The UVC standard does not support the Raw format. For RAW8 - RAW12, the input data is captured in 16bit width and output to PC. Unconnected bits are indeterminate values, so it is recommended to use an external pull-down or pull-up.

When capturing in RAW format, specify UYVY in the pixel format settings so that the data is packed as 16bit /pixel, and perform RAW image processing on the host PC software. Additionally, SVMCtl allows the RAW input to be output as a monochrome YUV 8bit format through its configuration settings.



For RAW20, the input data is assumed to be 24bit width and output to the PC. Specify RGB24 in the pixel format setting to pack the image into 24bit / pixel, and then process the RAW image using the host PC software.



On the host side, it is treated as RGB24, and the upper bit are padded with 0. (Bit rate is 6/5 times)

For board settings at the Raw input, also see “SVMCtl Software Manual”.

2.7. FSYNC Output Setting

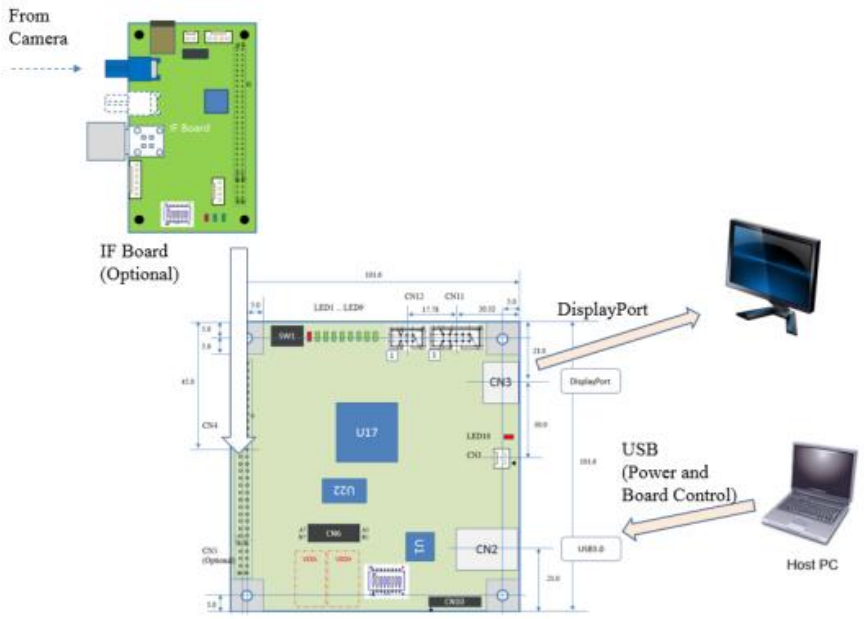
FSYNC can be output from P3 (GPIO 9) based on the configuration in the PC software SVMCtl. For details on how to configure FSYNC and its specifications, refer to the SVMCtl software manual.

3. DisplayPort Mode Operation Details

This section describes DisplayPort mode (Parallel input / DisplayPort output).

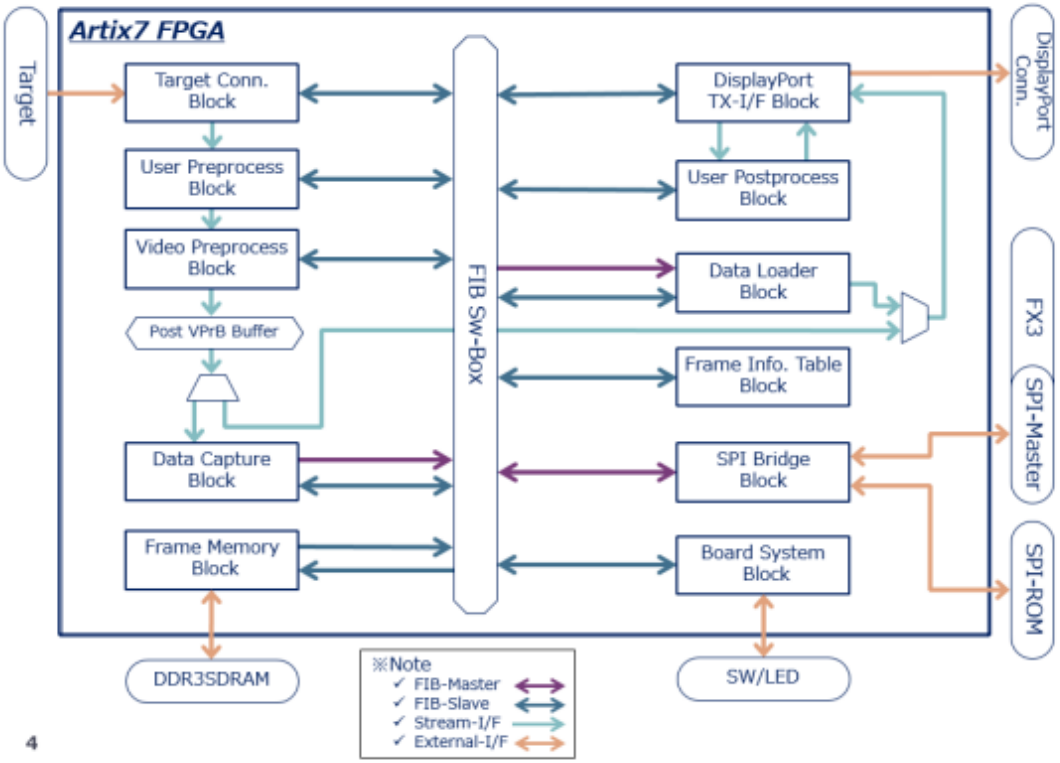
The SVP-01-UVC starts in DisplayPort mode when powered on with DIP switch settings #7 = OFF and #8 = OFF.

3.1. Connection Configuration Example of DisplayPort Mode



- For initial board settings, I2C setting and power supply, the USB connector is used.
- This board can operate with supplied +5V from CN1. In this case, the USB connector does not need to be connected.
- DisplayPort output and USB output cannot be used at the same time.

3.2. FPGA Internal Block Diagram in DisplayPort Mode



3.3. Format Setting

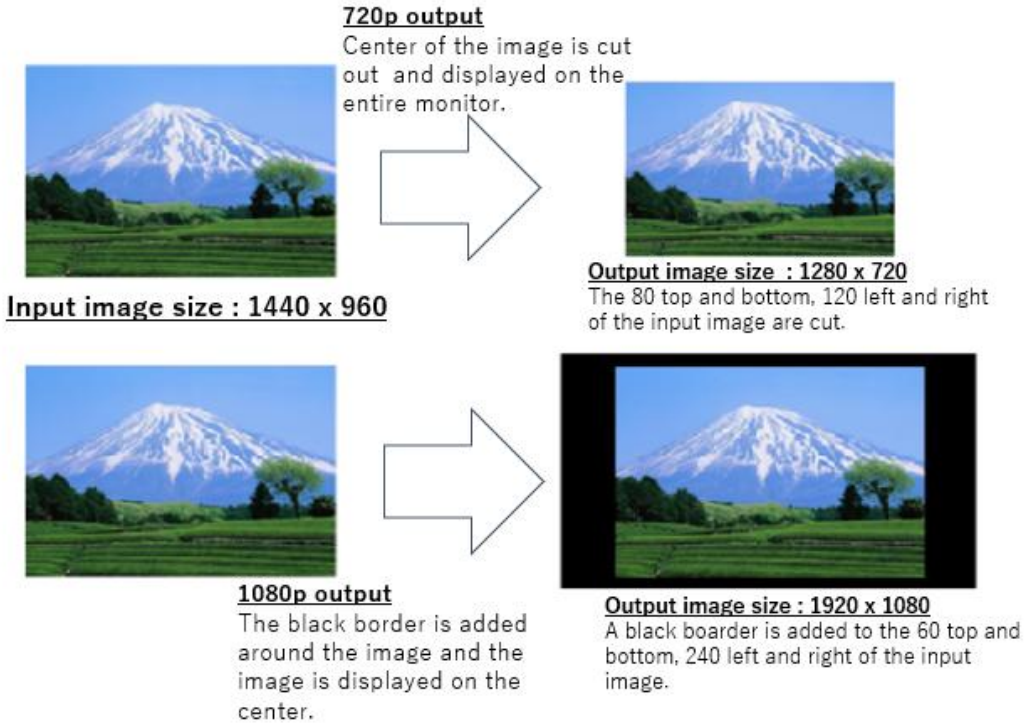
In DisplayPort mode, the required configuration items are the resolution, frame rate, output pixel format settings, and synchronization signal settings. These settings are written via the USB connector with SVMCtl. Once the initial setting has been completed, no further setting is required from the second startup onward.

Set the resolution and frame rate according to the specifications of the input video signal. When outputting only a specific region of the input image, configure the clipping settings. If clipping is enabled, the resolution setting in SVMCtl must be set to the resolution after clipping is applied.

This board does not have a scaling function. If the input resolution is smaller than the output one, add a black border around it. If the input resolution is larger than the output one, it is clipped in the center. The extraction position can also be specified through the clipping settings.

For parallel video signals, the polarity of the synchronization signal must be set appropriately. On this board, the polarities of VSYNC, HSYNC, and DE (when used)

can be configured as needed. When inputting embedded sync signals in the BT.656 format, enable the embedded sync setting.



The input signal bus width is configured to 8bit - 32bit using the DIP switch settings on the board. For RGB24 input, set the bus width to 24bit / pixel.

3.4. Raw Input Processing

When inputting a Raw image sensor signal, there is no Bayer -> Color conversion function in the DisplayPort mode. However, it is possible to output a monochrome image in a dot-by-dot format, with one pixel output per input pixel. In this case, only the upper 8bits are output, so when inputting signals with a bit width of RAW10 or higher, the lower bits are discarded.

To output a monochrome image, the bit shift and Raw processing settings must be written to the board using SVMCtl. If these settings are not applied, the input data is processed as YUV signals and will not be displayed correctly.

3.5. Custom Resolution

By setting DIP switch #4 to ON, output resolutions other than 1920 x 1080 and 1280 x 720 (custom resolutions) can be selected.

When outputting an image at a custom resolution, the timing of the output video signal can be specified in pixel-clock units. By writing timing data (.svo) to the on-board SPI-ROM from SVMCtl, the board operates in the user-defined timing output mode. If no timing data is written to the SPI-ROM, custom resolution output is disabled.

When using the custom resolution feature, a manual for creating timing data (.svo) is not currently available. Please contact us with the desired output resolution, frame rate, and pixel clock.

3.6. Color Conversion Formula

The RGB, YUV conversion formula follows bt.601. Input / output scaling (Limited / Full conversion) can be configured using SVMCtl. In the default state, no scaling is applied to either the input or the output.

4. Board External and Dimensions

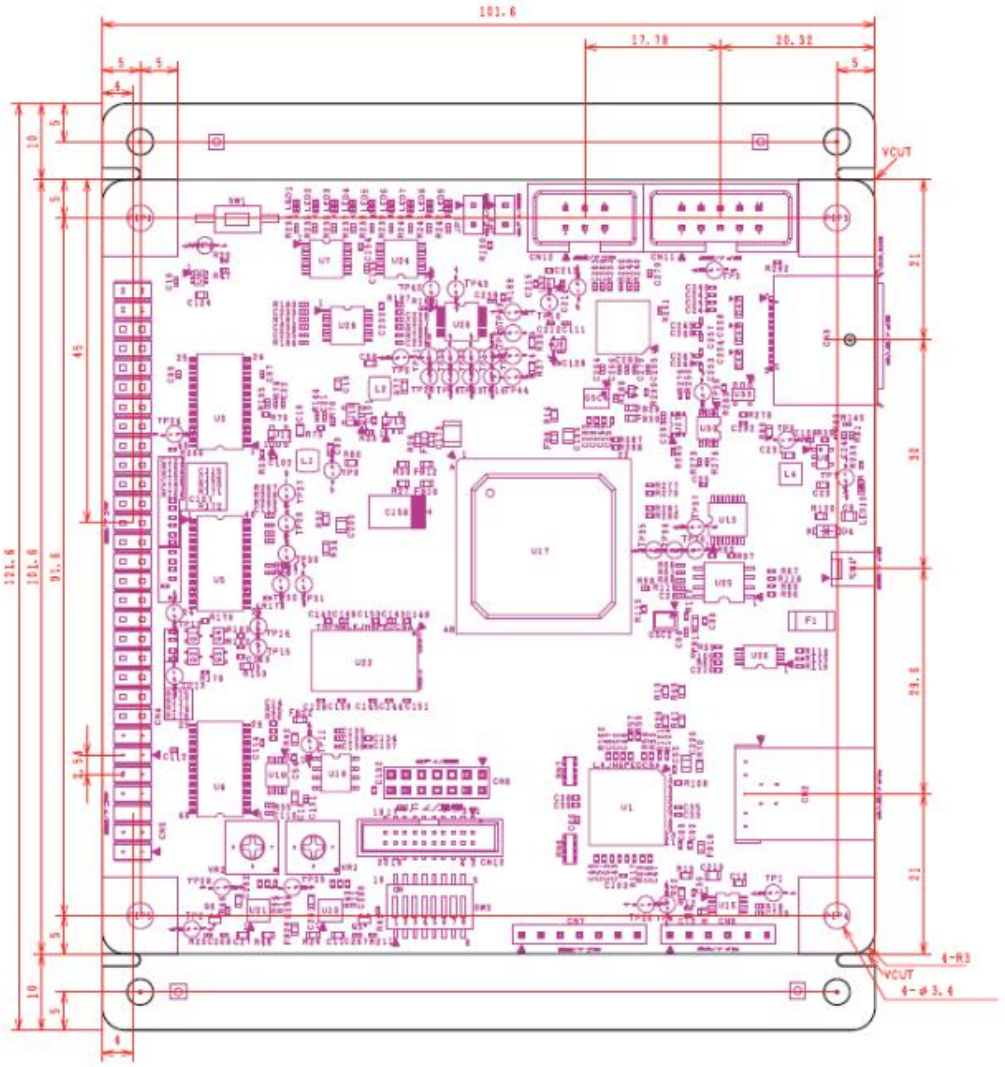
The photo and diagram of the SVP-01-UVC are shown below.

4.1. Board Photo

- Depending on the lot, the mounting state of the parts may be different.
- SVP-01-UVC, SVP-01-GEN and SVP-01-VND are using same board, but the firmware is different. Refer to the label on the back of the board for the board type.

4.2. Drawing

The top and bottom 10mm are discarded plates. It does not attach the board.



5. Connector Specification

This chapter describes the connector specifications that should be considered when connecting to a camera or during normal use.

5.1. Connector List

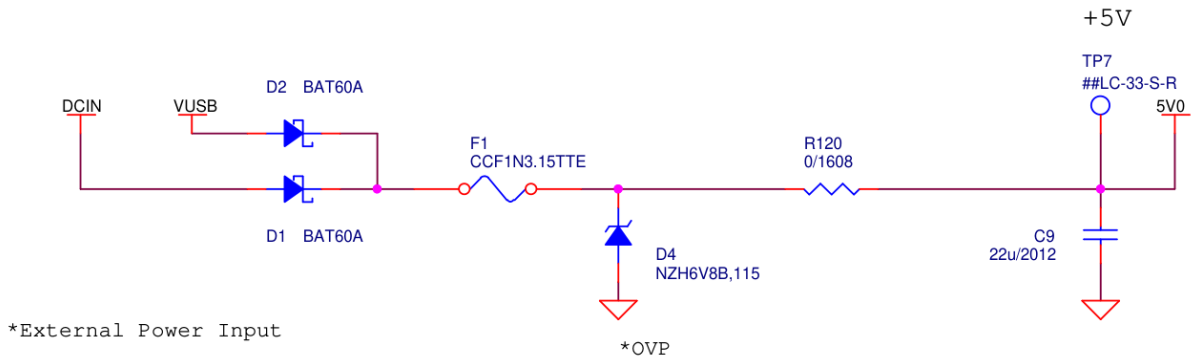
CN#	Mounted State	Model number	Function
CN1		22-04-1021	Sub power connector
CN2		1003-024-02000	USB3.0 type-B connector
CN3		0472720001	DisplayPort connector
CN4		PRPC025DAAN-RC	Parallel signal input / output (1-50P)
CN5	Un-mounted	PRPC005DAAN-RC	Parallel signal input / output (51-60P)
CN6		0877581416	JTAG connector
CN7	Un-mounted	A2-7PA-2.54DSA	(For debug)
CN9	Un-mounted	A2-6PA-2.54DSA	(For debug)
CN10	Un-mounted	A2-6PA-2.54DSA	(For debug)
CN11	Un-mounted	87834-1019	For synchronous wiring connector (5x2)
CN12	Un-mounted	87834-0619	For synchronous wiring connector (3x2)
CN13		3220-20-0300-00	For shipping check connector

- The mounted state is standard specifications of the SVP-01-UVC.
- CN6 - CN13 don't use normally.
- CN5 is used when expand the bit width of the parallel signals.

5.2. CN1: Sub Power Connector

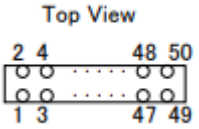
This power connector is used when the USB bus power cannot meet the power capacity.

Connector		22-04-1021: Molex					
Pin #	Signal	Direction	Note	Pin #	Signal	Direction	Note
1	+5V	IN	DC5V power input	2	GND	-	Power ground



- The power input of CN1, the VBUS (VUSB) of CN2, and the VBUS (VBUS_2) of CN3 are connected by diode OR as shown in the above figure.
- Input voltage range is 4.75V ~ 5.5V.

5.3. CN4: Target Connection Connector A



This connector connects to the target image sensor, and is a pin header with a pitch of 2.54mm.

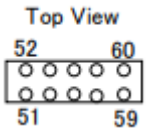
It can be connected using a general pin socket or IDC cable. Image sensors with a bit width of 24bit - 32bit are used by combining CN4 and CN5.

Connector		PRPC025DAAN-RC					
Pin #	Signal	Direction	Note	Pin #	Signal	Direction	Note
1	VDDL	OUT	IO voltage level output (1.8-3.3V)	2	GND	-	-
3	P0	IN	General purpose input port 0 / Pixel_DATA16	4	GND	-	-
5	P1	IN	General purpose input port 1/ DE input (8-16bit) / Pixel_DATA17	6	GND	-	-
7	P2	IN	General purpose input port 2 / Pixel_DATA18	8	GND	-	-
9	P3	OUT / IN	FSYNC output port	10	GND	-	-
11	P4	OUT / IN	General purpose output port 1 / DE input (24bit) / Pixel_DATA25	12	HSYNC	IN	Horizontal synchronization input
13	VSYNC	IN	Vertical synchronization input	14	XRST	OUT	Reset signal output
15	VDDH	OUT	Target power output (1.2V - 3.6V can be set)	16	GND	-	-
17	SDA	IO	I2C_DATA	18	GND	-	-
19	SCL	IO	I2C_CLK	20	GND	-	-

21	DCK	IN	Pixel_CLK (Pixel clock input)	22	GND	-	-
23	Y0	IN	Pixel_DATA0	24	GND	-	-
25	Y1	IN	Pixel_DATA1	26	GND	-	-
27	Y2	IN	Pixel_DATA2	28	GND	-	-
29	Y3	IN	Pixel_DATA3	30	GND	-	-
31	Y4	IN	Pixel_DATA4	32	GND	-	-
33	Y5	IN	Pixel_DATA5	34	GND	-	-
35	Y6	IN	Pixel_DATA6	36	GND	-	-
37	Y7	IN	Pixel_DATA7	38	GND	-	-
39	CLKOUT	OUT	Target drive clock	40	GND	-	-
41	Y8	IN	Pixel_DATA8	42	Y9	IN	Pixel_DATA9
43	Y10	IN	Pixel_DATA10	44	Y11	IN	Pixel_DATA11
45	Y12	IN	Pixel_DATA12	46	Y13	IN	Pixel_DATA13
47	Y14	IN	Pixel_DATA14	48	Y15	IN	Pixel_DATA15
49	3V3	OUT	3.3V Output	50	P5	OUT / IN	General purpose output port 2 / Pixel_DATA26

5.4. CN5: Target Connection Connector B

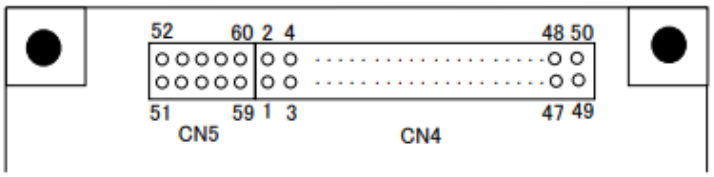
This connector connects to the target.



Connector		PRPC005DAAN-RC					
Pin #	Signal	Direction	Note	Pin #	Signal	Direction	Note
51	P6	OUT / IN	General purpose output port 3 / Pixel_DATA27	52	P7	OUT / IN	General purpose output port 4 / Pixel_DATA28
53	P8	OUT / IN	General purpose output port 5 / Pixel_DATA29	54	P9	OUT / IN	General purpose output port 6 / Pixel_DATA30
55	P10	OUT / IN	General purpose output port 7 / Pixel_DATA31	56	P11	IN	General purpose input port 3 / Pixel_DATA19
57	P12	IN	General purpose input port 4 / Pixel_DATA20	58	P13	IN	General purpose input port 5 / Pixel_DATA21
59	P14	IN	General purpose input port 6 / Pixel_DATA22	60	P15	IN	General purpose input port 7 / Pixel_DATA23

- CN5 is optional. The pin header is not mounted on SVP-01-UVC standard version.
- The input / output direction of Pixel_DATA [31:24] is changed depending on input bit width setting.

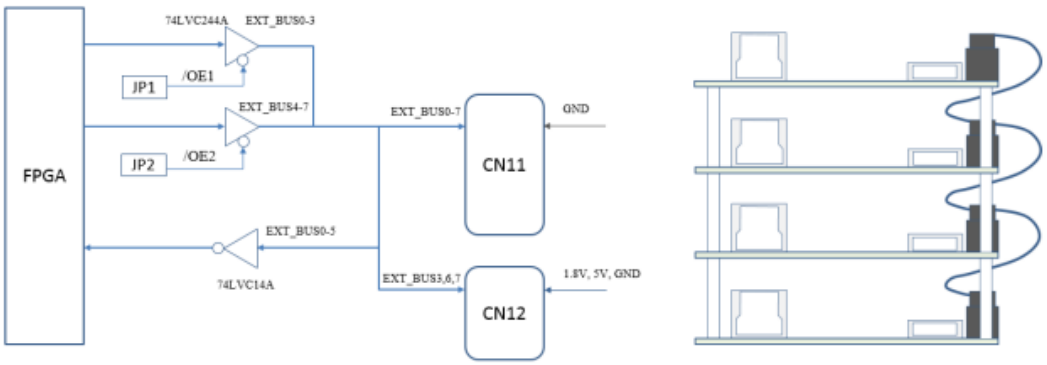
5.5. Relative Positions of CN4 and CN5



- CN4 and CN5 can be used together as a 60pin header.

5.6. CN11, CN12: Connector for Synchronous Wiring

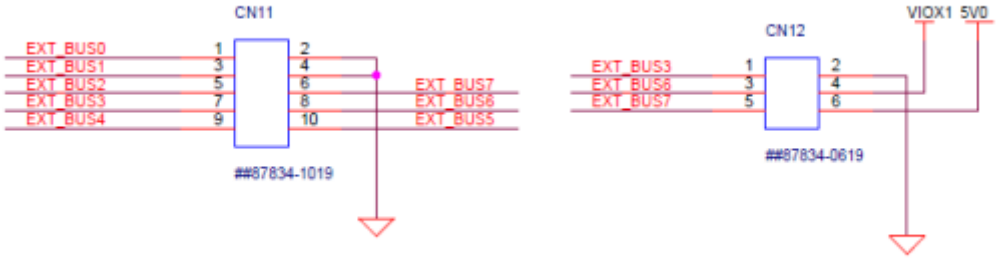
CN11 and CN12 are connectors used for synchronization wiring between boards, and a 2.54mm pitch IDC connector can be used to connect the boards. As a custom feature, multiple SV series boards can be connected through these connectors to enable functions such as capture synchronization and timestamping. These connectors are not used in the standard specification (they are reserved for future feature expansion).



(Block Diagram)

When the JP1 is shorted, the EXT_BUS0-3 signal line becomes output. When JP2 is shorted, the EXT_BUS4-7 signal line becomes output.

(Pin Assignment)



5.7. Configuration Table of Input Data

When connecting a YUV format or RGB24 format image sensor to the SVP-01-UVC, wire the signals according to the table below.

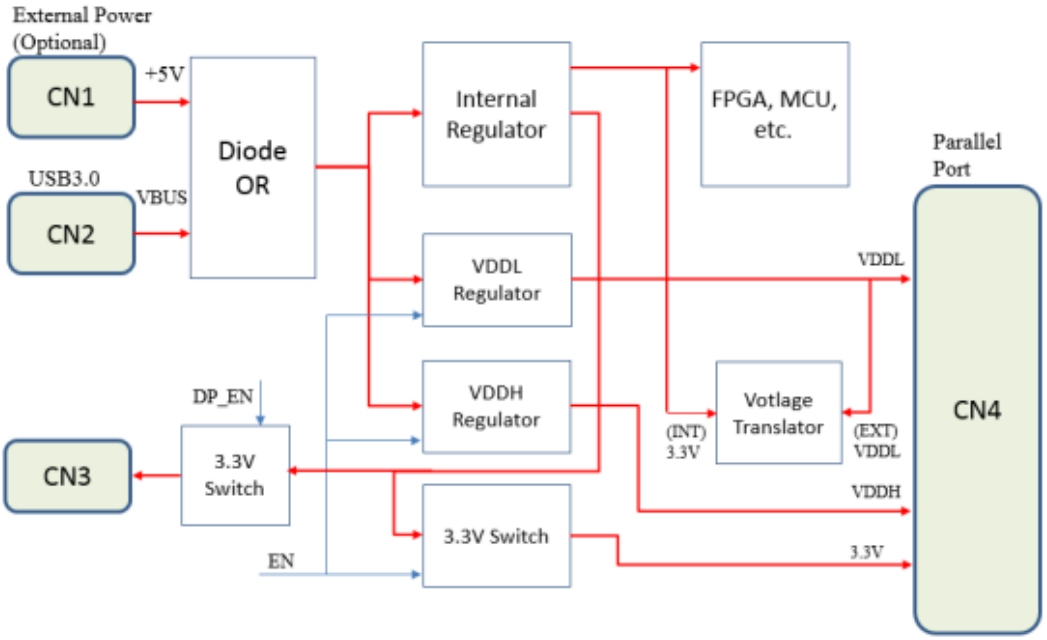
Format	YUV4:2:2			RGB24
Bit Width	8bit (UYVY/YUY2)	16bit (UYVY)	32bit (UYVY)	24bit
Pixel_DATA [31:24]	-	-	V	-
Pixel_DATA [23:16]	-	-	Y	R
Pixel_DATA [15:8]	-	U, V	U	B
Pixel_DATA [7:0]	Y, U, V	Y	Y	G

- The polarities of VS, HS, and the clock signal can be configured as needed.

6. Details of Each Part

6.1. Power Supply System

The power supply system of this board shown below. The board power supply can be operated by USB power supply or external +5V. Some of the internal regulator outputs are connected to CN4, and the connected device can also operate with USB power supply.



6.2. SW1: Push Switch

SW1 is a switch for functions such as controlling the reset output signal line and sending the initial settings to the I2C bus. The function of SW1 can be modified through SVMCtl. For details, refer to the SVMCtl software manual.

6.3. SW2: DIP Switch

These are 8bit switches for setting various operating modes. Depending on the operating mode, the following settings are available.

6.3.1. UVC Mode

No.#	Item	OFF	ON
1	Camera input bit width setting 1 (When #3=OFF)	8bit x 2 CLK	16bit x 1 CLK (YUV) or 24bit x 1 CLK (RGB)
2	Test pattern output	Standard operation	Test pattern output
3	Camera input bit width setting 2	(Following DIP switch #1)	32bit x 1/2 CLK
4	-	-	-
5	-	-	-
6	-	-	-
7	Operation mode setting (When start up)	7:ON, 8:OFF: Updater mode 7:OFF, 8:ON: UVC mode 7:OFF, 8:OFF: DisplayPort mode 7:ON, 8:ON: Reserved	
8			

#4 and #6 are reserved for future functions. Normally, these switches should be set to OFF.

6.3.2 DisplayPort Mode

No.#	Item	OFF	ON
1	Camera input bit width setting 1 (#3=OFF)	8bit x 2 CLK	16bit x 1 CLK (YUV) or 24bit x 1 CLK (RGB)
2	Test pattern output	Standard operation	Test pattern output
3	Camera input bit width setting 2	(Following DIP switch #1)	32bit x 1/2 CLK
4	Select custom resolution	Standard operation (Resolution specified by DIP switch #5,6)	Custom resolution output (Specified in SVMCtl)
5	Monitor output format setting	ON: RGB888 output OFF: YUV422 8-bit output	

6	Monitor output resolution setting	ON: 720p (1280 x 720) OFF: 1080p (1920 x 1080)
7	Operation mode setting (When start up)	7:ON, 8:OFF: Updater mode 7:OFF, 8:ON: UVC mode 7:OFF, 8:OFF: DisplayPort mode 7:ON, 8:ON: Reserved
8		

- When "Monitor output format setting" is ON, the video data is converted to RGB format and output to DisplayPort. When it is OFF, video data is output to DisplayPort in YUV format.
- The default frame rate for DisplayPort output is 60fps. However, if the custom resolution settings are not written to the board, setting DIP switch #4 = ON will result in 30fps output.
- DIP switch #5 = OFF (YUV422 output) may not be supported with all monitors. If your monitor does not support it, change it to RGB888 and output it, but the color will not be reproduced correctly. If the video is not displayed correctly on the monitor, set #5 = ON (RGB output).
- For RGB888 input, set DIP switch #1 = ON and configure the Color Space setting in SVMCtl to RGB888.

6.4. LED1-10: Operating Status

These LEDs display the operating status of such as board and FPGA.

LED#	Explanation
1	When the power is being supplied to the target, light up. This is a red LED.
2	When the clock supplied to the target is locked, light up.
3	When the synchronization signal for video input from the target is detected, light up.
4	This light turns ON/OFF at the cycle of the VSYNC synchronization signal from the target divided by 3. If the input image is 30 fps, it repeats flashing 5 times per second.
5	(DisplayPort mode) <Reserved> (UVC mode) When a frame drop occurs due to a delay in USB transfer and a buffer overflow, light up. A reset is triggered when preview is started in the capture software (NVCap).

6	<Reserved>
7	<Reserved>
8	(DisplayPort mode) <Reserved> (UVC mode) This light turns on during capture from the host PC via USB.
9	(DisplayPort mode) This light turns ON/OFF at the cycle of the VSYNC synchronization signal to the DisplayPort monitor output divided by 3. If the output image is 60 fps, it repeats flashing 10 times per second. (UVC mode) This light flash at a cycle by dividing the FV (Frame Valid) pulse of the UVC output from the Main port by 3.
10	When the power is being supply to the board, light up. This is a red LED.

- LEDs marked as <Reserved> in the table will be assigned for future function. In the current version, these LEDs change their lighting state depending on the state inside the board.
- When the I2C setting is being sent, the LED1-8 flash at high speed.
- If the license key has not been written to the board, LED1-8 will light up in order at low speed.
- During the DisplayPort connection process in the DisplayPort mode, LED1-6 are light up in order depending on the state. After the connection process is complete, it will be returned to the original state.
- If the board stops due to USB error, all LED will flash at low speed at the same time.

6.5. VR1, VR2: Connectors for Adjusting VDDH and VDDL

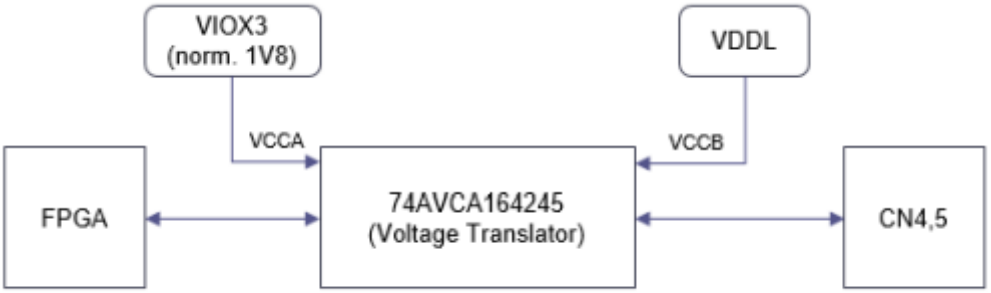
These are variable resistors for adjusting the power supply for the target device generated by SVP-01-UVC. VDDL can be adjusted in the range of 1.8V - 3.3V and VDDH in the range of 1.2V - 3.6V.

The VDDL is connected to the translator IC, and the voltage level of the parallel video input signal and general input / output are the VDDL voltage. The VDDL must be set according to the target.

On the other hand, the VDDH output to only the connector and is not used inside the board. It can be used as the power supply for the target.

The VDDL and VDDH are set to 3.3V at the time of shipment. Before use, adjust the setting to match the target side voltage.

6.6. CN4,5 Input / Output Circuit Schematic Diagram



- The I/O voltage of each single-ended I/O pin on the CN4 and CN5 side is determined by the VDDL voltage.

6.7. Operating Temperature Range

The operating temperature range of the IC on this board is 0-80℃. However, this value is not considered about the heat generation of the device.

Therefore, when the board is operating, the ambient temperature (the operating temperature range) should be 0-42°C in UVC mode and 0-36°C in DisplayPort mode. We have confirmed that it works even at temperatures higher than this (60°C), but we cannot guarantee it.

If you want to operate it in a higher temperature or if you put it into a case, it is recommended to attach a suitable heat sink to the FPGA or cool it with a fan.

For reference, if the heat sink LPD25-15B (25 x 25 x 15mm) is attached to the FPGA and cools in an open space, the upper operating temperature limit calculated in the same way is 55°C in UVC mode and 49°C in DisplayPort mode (measured value by our company).

7. Applicable Version

This document supports the following versions.

Mode	FX3 Version	FPGA Version
Updater mode	After 117	After 0.20
UVC mode	After 133	After 1.06
DisplayPort mode	After 133	After 1.08
SVMCtl	After v1.7.8.1	
SVMUpdater	After v1.8.0.9	

8. Precaution

When using this board, please observe the following precautions.

1. When updating the FW / FPGA, set the DIP switch (SW2) #7 = ON, #8 = OFF and use update software (SVMUpdater) on the host PC.
2. When connecting or disconnecting the target device, such as an interface board, make sure the board is powered off.
3. Connecting a device to the interface board or to the DisplayPort requires additional current consumption. Use a power supply with sufficient current capacity for powering this board.
4. The contents of this document may change without advance notice.
5. We have made every effort to ensure that the contents of this document are complete, but if you notice any suspicious points, errors, omissions, etc., please contact to sv-support@net-vision.co.jp.
6. Be sure to use SVMCtl and SVMUpdater versions released after the launch of the SVP-01-UVC (Aug. 2022). Use SVMCtl v1.4.7.2 or later, and use SVMUpdater v1.7.3.0 or later. Using older software versions to update or configure this board may prevent the SVP-01-UVC from being recognized by the software, which can result in improper operation.